

AD-A183 596 DIGITALLY PROGRAMMABLE ACTIVE SWITCHED CAPACITOR
FILTERS(U) NAVAL POSTGRADUATE SCHOOL MONTEREY CA
C YALKIN MAR 87

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THESIS

DIGITALLY PROGRAMMABLE
ACTIVE
SWITCHED CAPACITOR FILTERS

by

Yalkin, Cengiz

March 1987

Thesis Advisor

Sherif Michael

AUG 21 1987

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87 8 13 011

REPORT DOCUMENTATION PAGE

1a REPORT SECURITY CLASSIFICATION UNCLASSIFIED			1b RESTRICTIVE MARKINGS		
2a SECURITY CLASSIFICATION AUTHORITY			3 DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution is unlimited		
2b DECLASSIFICATION/DOWNGRADING SCHEDULE			5 MONITORING ORGANIZATION REPORT NUMBER(S)		
4 PERFORMING ORGANIZATION REPORT NUMBER(S)			7a NAME OF MONITORING ORGANIZATION Naval Postgraduate School		
6a NAME OF PERFORMING ORGANIZATION Naval Postgraduate School		6b OFFICE SYMBOL (if applicable) 62	7b ADDRESS (City, State, and ZIP Code) Monterey, California 93943-5000		
6c ADDRESS (City, State, and ZIP Code) Monterey, California 93943-5000		9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER			
8a NAME OF FUNDING/SPONSORING ORGANIZATION		8b OFFICE SYMBOL (if applicable)	10 SOURCE OF FUNDING NUMBERS		
8c ADDRESS (City, State, and ZIP Code)		PROGRAM ELEMENT NO	PROJECT NO	TASK NO	WORK UNIT ACCESSION NO
11 TITLE (Include Security Classification) DIGITALLY CONTROLLED PROGRAMMABLE ACTIVE SWITCHED CAPACITOR FILTERS(U)					
12 PERSONAL AUTHOR(S) Yalkin, Cengiz					
13a TYPE OF REPORT Master's Thesis		13b TIME COVERED FROM _____ TO _____		14 DATE OF REPORT (Year, Month, Day) 1987 March	
15 PAGE COUNT 89					
16 SUPPLEMENTARY NOTATION					
17 COSATI CODES			18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number)		
FIELD	GROUP	SUB-GROUP	digitally controlled filter, bilinear realization of a resistance,		
19 ABSTRACT (Continue on reverse if necessary and identify by block number)					
<p>In this research, analog active circuits are analyzed and designed using periodic sampling techniques. Switched capacitor networks are the basis of these techniques. The use of switched capacitor network allows active filters to be implemented in IC form. As an application, a general purpose digitally controlled analog sampled data filter is presented. The results of this programmable filter are compared with the computer simulations for theoretical and practical verifications. The final goal of this research is to demonstrate a number of practical conclusions about switched capacitor networks.</p>					
20 DISTRIBUTION/AVAILABILITY OF ABSTRACT <input checked="" type="checkbox"/> UNCLASSIFIED/UNLIMITED <input type="checkbox"/> SAME AS RPT <input type="checkbox"/> DTIC USERS			21 ABSTRACT SECURITY CLASSIFICATION unclassified		
22a NAME OF RESPONSIBLE INDIVIDUAL Sherif Michael			22b TELEPHONE (Include Area Code) 408-646-2252		22c OFFICE SYMBOL 62Mi

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Digitally Programmable
Active
Switched Capacitor Filters

by

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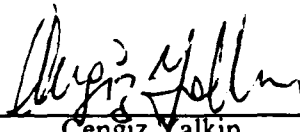
Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

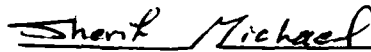
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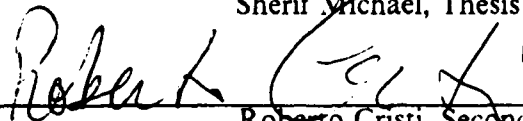
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ABSTRACT

In this research, analog active circuits are analyzed and designed using periodic sampling techniques. Switched capacitor networks are the basis of these techniques. The use of switched capacitor network allows active filters to be implemented in IC form. As an application, a general purpose digitally controlled analog sampled data filter is presented. The results of this programmable filter are compared with the computer simulations for theoretical and practical verifications. The final goal of this research is to demonstrate a number of practical conclusions about switched capacitor networks.



TABLE OF CONTENTS

I.	INTRODUCTION	10
A.	WHY SWITCHED CAPACITORS?	10
B.	NOTATION	10
C.	SWITCHED CAPACITOR EQUIVALENT RESISTORS	12
D.	CHARGE CONSERVATION ANALYSIS	16
E.	EXPERIMENTAL DEMONSTRATION OF SWITCHED CAPACITOR AS EQUIVALENT RESISTOR	17
F.	NONIDEAL PROPERTIES OF THE SWITCHED CAPACITOR	22
II.	THE BILINEAR TRANSFORMATION AS A SC FILTER DESIGN TECHNIQUE	25
A.	GENERAL	25
B.	BILINEAR TRANSFORMATION	26
C.	THE EFFECTS OF HIGH SAMPLING RATE	29
D.	ELEMENT TRANSFORMATIONS	32
	1. Capacitor	32
	2. Resistor	33
	3. Inductor	33
E.	INTEGRATORS USING BILINEAR TRANSFORMATION	36
	1. Lossless Integrator	36
	2. Lossy Integrator and Experimental Results	38
III.	PROGRAMMABLE GIC SC FILTER	45
A.	GENERAL	45
B.	THE PROPOSED GIC SC PROGRAMMABLE FILTER	45
C.	THE REALIZED GIC SC PROGRAMMABLE FILTER	47
IV.	COMPUTER SIMULATION OF THE PROPOSED GIC ACTIVE FILTER	58
A.	INTRODUCTION	58

B.	SIMULATION RESPONSE(S)	58
1.	Low Pass Filter Realization	58
2.	High Pass Filter Realization	59
3.	Band Pass Filter Realization	62
4.	Notch Filter Realization	64
5.	All Pass Filter Realization	66
V.	EXPERIMENTAL RESULT OF THE PROGRAMMABLE GIC SC FILTER	68
A.	GENERAL	68
B.	LOW PASS FILTER	68
C.	HIGH PASS FILTER	71
D.	BAND PASS FILTER	74
E.	NOTCH FILTER	76
F.	ALL PASS FILTER	77
G.	EFFICIENCY OF THE CLOCK FREQUENCY	77
VI.	CONCLUSION	80
	APPENDIX A: TRANSFORMATION PROGRAM	81
	APPENDIX B: SIMULATION PROGRAM	82
	LIST OF REFERENCES	87
	INITIAL DISTRIBUTION LIST	88

LIST OF TABLES

1.	THE ELEMENTS IDENTIFICATION FOR DIFFERENT REALIZATIONS OF THE GIC FILTER	47
2.	THE TRUTH TABLE OF THE SWITCHES LOGIC USED TO SELECT THE FILTERING FUNCTION	48
3.	THE FOUR-BIT WORDS THAT CONTROL W_p (F_p)	54
4.	THE FOUR-BIT WORDS THAT CONTROL Q_p	55

LIST OF FIGURES

1.1	Waveforms of a Two-Phase Clock	11
1.2	The Parallel SC Resistor Realization	12
1.3	The Series SC Resistor Realization	14
1.4	The Combination of the Parallel and Series Realization	15
1.5	The Bilinear SC Realization of a Resistor	16
1.6	The Two Phase Clock Circuit	18
1.7	Two-Phase Clock	19
1.8	Leading Edge	19
1.9	Falling Edge	19
1.10	Experimental Circuit Using Parallel SC Realization	20
1.11	Experimental Result of Parallel SC Realization	21
1.12	Experimental Result of Parallel SC Realization	21
1.13	Experimental Circuit Using Bilinear SC Realization	23
1.14	Experimental Result of Bilinear SC Realization	23
1.15	Experimental Result of Bilinear SC Realization	23
1.16	Appearing of the Parasitic Capacitance	24
2.1	Floating Capacitor	34
2.2	An Analog Integrator	36
2.3	Bilinear SC Integrator	37
2.4	Bode Plot for an Analog Integrator	39
2.5	Magnitude Response for the Bilinear SC Integrator	39
2.6	The Lossy Bilinear Integrator	40
2.7	Computer Simulation of Lossy Integrator in s-Domain (Magnitude)	41
2.8	Computer Simulation of Lossy Integrator in s-Domain (Phase)	41
2.9	Computer Simulation of Lossy Bilinear Integrator in z-Domain (Magnitude)	42
2.10	Computer Simulation of Lossy Bilinear Integrator in z-Domain (Phase)	42
2.11	Computer Simulation of Lossy Bilinear Integrator Using Building Blocks Approach (Magnitude)	43

2.12	Computer Simulation of Lossy Bilinear Integrator Using Building Blocks Approach (Phase)	43
2.13	Experimental Result of Lossy Bilinear Integrator	44
3.1	The GIC Implementation Using Op. Amps.	46
3.2	Schematic Diagram of the Programmable GIC SC Filter Showing the Controlled Nodes and Switches	48
3.3	The Detailed Design of the Control Circuit	49
3.4	The Two Capacitor Banks Realization for the Programming of w_p	51
3.5	The Capacitor Bank for the Programming of Q_p	52
3.6	The Detailed Design of Signal Processing Circuit	53
3.7	The Implemented Capacitor Bank for $w_p (f_p)$	56
3.8	The Implemented Capacitor Bank for Q_p	57
4.1	Ideal GIC LPF Magnitude Response	59
4.2	Ideal GIC LPF Magnitude Response	59
4.3	Ideal GIC LPF Magnitude Response	60
4.4	Ideal GIC LPF Magnitude Response with Different Q_p s	60
4.5	Ideal GIC HPF Magnitude Response	61
4.6	Ideal GIC HPF Magnitude Response	62
4.7	Ideal GIC HPF Magnitude Response	62
4.8	Ideal GIC HPF Magnitude Response with Different Q_p s	63
4.9	Ideal GIC BPF Magnitude Response	64
4.10	Ideal GIC BPF Magnitude Response	64
4.11	Ideal GIC BPF Magnitude Response with Different Q_p s	65
4.12	Ideal GIC NF Magnitude Response	66
4.13	Ideal GIC NF Magnitude Response with Different Q_p s	66
4.14	Ideal GIC AP Phase Response	67
5.1	Experimental Result of LPF with Different f_p	69
5.2	Experimental Result of LPF with Different f_p	70
5.3	Experimental Result of LPF with Different f_p	70
5.4	Experimental Result of LPF with Different Q_p	71
5.5	Experimental Result of HPF with Different f_p	72
5.6	Experimental Result of HPF with Different f_p	72
5.7	Experimental Result of HPF with Different f_p	73
5.8	Experimental Result of HPF with Different Q_p	73

5.9	Experimental Result of BPF with Different f_p	74
5.10	Experimental Result of BPF with Different f_p	75
5.11	Experimental Result of BPF with Different Q_p	75
5.12	Experimental Result of NF with Different f_p	76
5.13	Experimental Result of NF with Different Q_p	77
5.14	Experimental Result of AF with Different f_p	78
5.15	Experimental Result Showing the Effect of the f_c	79
5.16	Experimental Result Showing the Effect of the f_c	79

I. INTRODUCTION

A. WHY SWITCHED CAPACITORS?

Modern active filter design is based mainly on RC filters. Practical RC filter realizations require in most cases large-valued capacitors, and high precision resistors and capacitors components to achieve accurate time constant. These two features created a major obstacle for IC implementation of RC filters.

The MOS integrated-circuit technology had found wide usage in industry because of its superior logic density, as compared to that achievable with bipolar technologies. A unique property which is held by the MOS integrated-circuits is the capability to store charge on a node for a short period of time, order of milliseconds, and to sense this stored charge continuously and nondestructively. This property was first used in dynamic random-access memories and dynamic logic. In the last few years the analog signal processing development gained a lot of momentum using the property mentioned above.

As it will be explained in the next section of this chapter, the realization of the RC time constant can be well controlled in MOS technology by determining clock period and the capacitor ratio. This idea made it possible for active filters to be implemented in IC form. Furthermore, MOS capacitors are nearly ideal, with very low dissipation factors and good temperature stability. As an economical approach, sampled-data filters can be fabricated using memory-like NMOS and CMOS processing. This analog and digital circuitry can be placed on the same chip. For the reasons presented above switched capacitor filters became attractive and useful.

B. NOTATION

In general sense, a switched capacitor network (SC) would be made up of switches, driven by an external clock, capacitors, and OP-amp if it is needed.

It is appropriate to identify some of the notations and symbols that will be used throughout this thesis. The switch symbol will always be shown open. It is said that the system has an n-phase clock, if the period of clock, T, has n segments corresponding to each phase. For simplicity, a two-phase clock is going to be used. Each switch associated with the proper clock phase will be designated by the symbol

$$\Phi_k$$

where k is an integer representing the number of clock phases in the system. Typically a switch is closed only once during the clock period. It is very important in SC networks to ensure that at any time, no two switches driven by different clock phases will be closed simultaneously (short circuit). Therefore, each phase of the clock has to have a less than 50% duty cycle. This is known as the *nonoverlapping clock*. Bipolar two phase nonoverlapping clock is shown in Figure 1.1. A convenient complementary notation for the clock phases is denoted by *odd* defined as Φ_1 and *even*, defined as Φ_2 . Thus, the sampled data waveforms can be stated as the sum of their odd and even components, e or o .

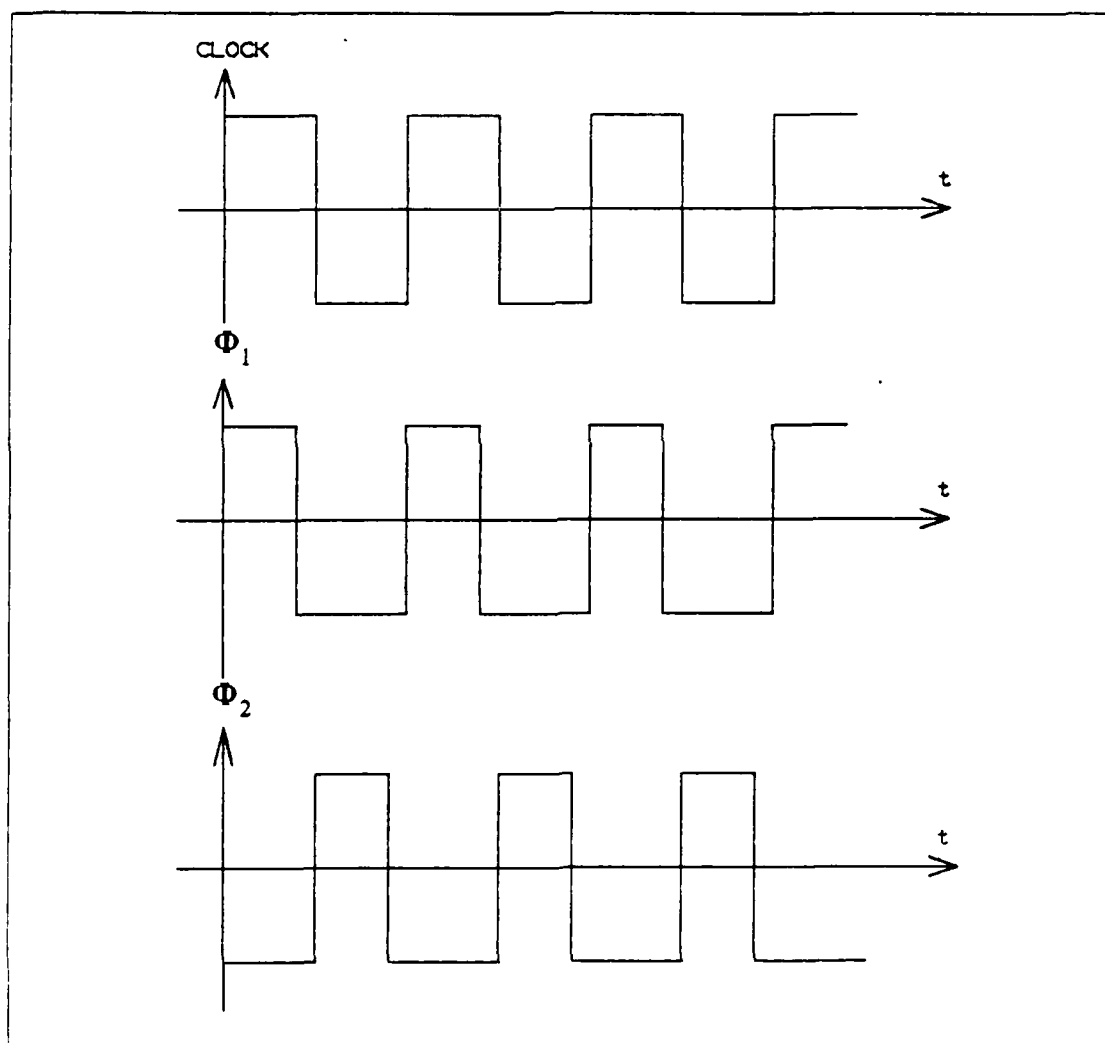


Figure 1.1 Waveforms of a Two-Phase Clock.

If we want to express the transfer function of a SC network, we can write at least four transfer functions corresponding to even and odd phase. A useful notation for the transfer function is shown in Equation 1.1; where i and j can be either e or o .

$$H^{ij}(z) = \frac{V_o^j(z)}{V_{in}^i(z)} \quad (\text{eqn 1.1})$$

Since the switched capacitor networks have sampled data character, they can be treated similar to digital filters and analyzed in z -domain. However, SC filters are analog networks; thus, the analog concepts of impedance and loading, which are absent in digital filters, are retained. To solve this problem and to be able to apply network theory, z -domain equivalent circuits, are used, (also known as building blocks).

C. SWITCHED CAPACITOR EQUIVALENT RESISTORS

In this section realization of continuous resistor will be denoted in several methods using switched capacitor networks. The main goal here is to have the ability to replace the continuous resistor using an equivalent SC realization. Several methods are developed for continuous resistor realization. Four of these realizations are discussed below. First, is the parallel switched capacitor resistor realization. In this method, the circuit in Figure 1.2 is considered.

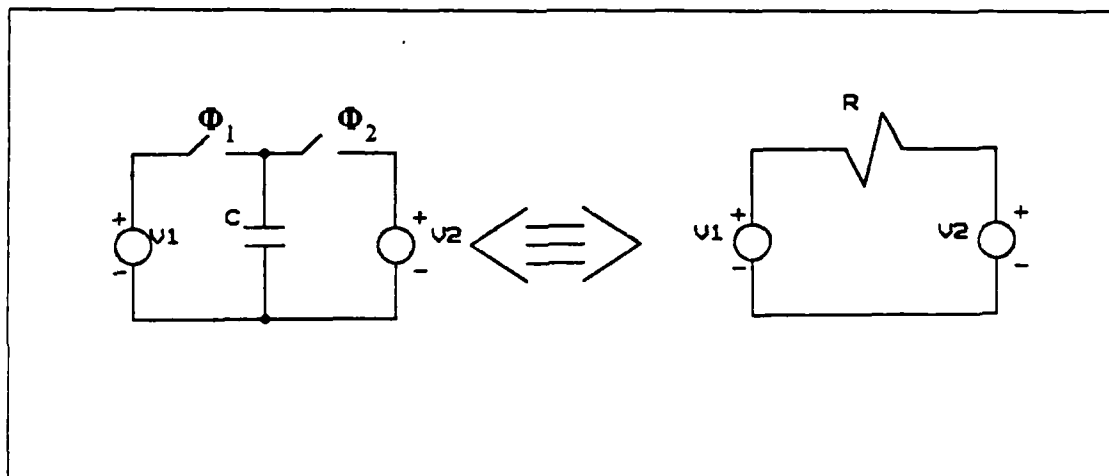


Figure 1.2 The Parallel SC Resistor Realization.

Initially, both switches are open and the capacitor is completely discharged. In the odd phase, Φ_1 is closed and capacitor will be charged to V_1 this can be expressed in the following

$$Q(t_0 + T/2) = CV_1 \quad (\text{eqn 1.2})$$

Because of the nonoverlapping clock, first Φ_1 will be open and then even phase will start, Φ_2 will be closed, and C will be charged to V_2 . In this phase, total charge on the capacitor is

$$Q(t_0 + T) = CV_2 - CV_1 \quad (\text{eqn 1.3})$$

We note that the final charge on the capacitor during one phase period is not necessarily equal to the charge flowing past the voltage sources during that period. The current can be written as

$$i = dq/dt \quad (\text{eqn 1.4})$$

$$dq = CdV \quad (\text{eqn 1.5})$$

$$dq = C(V_2 - V_1) \quad (\text{eqn 1.6})$$

on the average

$$I = \frac{C(V_2 - V_1)}{T} \quad (\text{eqn 1.7})$$

$$\frac{V_2 - V_1}{I} = \frac{C}{T} \quad (\text{eqn 1.8})$$

This yields the following relationship for parallel realization

$$R = T/C$$

(eqn 1.9)

where T is the clock period.

Second, let us consider the circuit shown in Figure 1.3 called the series switched capacitor realization of the continuous resistor. Using the same previous calculations for parallel SC resistor realization we can obtain Equation 1.9 as equivalent resistance for this type of realization.

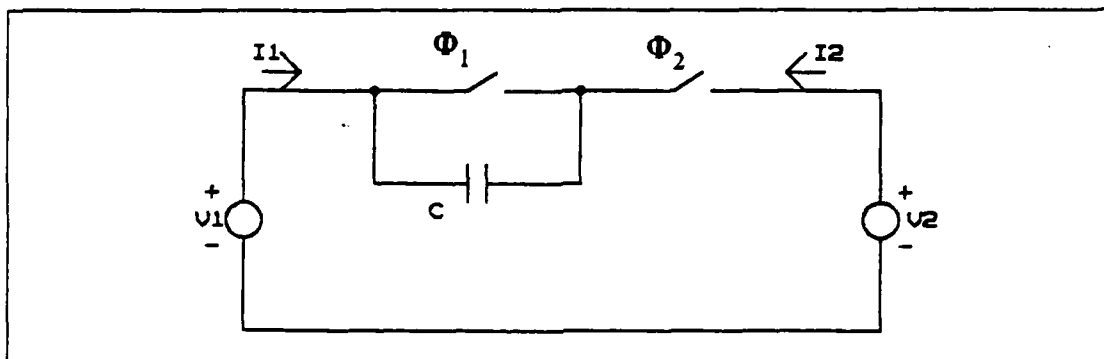


Figure 1.3 The Series SC Resistor Realization.

A third realization is a combination of the parallel and series realization. This type of circuit is shown in Figure 1.4. Initially, again, both capacitors are discharged and switches are open. In the odd phase, Φ_1 is closed and C_2 is charged to V_1 .

$$Q_1(t_0 + T/2) = C_2 V_1 \quad (\text{eqn 1.10})$$

In the even phase, Φ_1 is open and Φ_2 is closed respectively.

$$Q_2(t_0 + T) = C_1(V_2 - V_1) + C_2(V_2 - V_1) \quad (\text{eqn 1.11})$$

consequently

$$Q_1(t_0 + T) = C_1(V_1 - V_2) \quad (\text{eqn 1.12})$$

Equation 1.12 in fact is the component of $Q_2(t_0 + T)$ with the minus sign. If we continue to take the other phase, which is odd phase, we can write the following equation

$$Q_1(t_0 + 3T/2) = C_2(V_1 - V_2) \quad (\text{eqn 1.13})$$

So far, we completed one clock period, from $T/2$ to $3T/2$. Thus, we calculate the total charge going into voltage sources.

$$\begin{aligned} Q_1 &= \int_u^w i_1 dt = \int_u^v i_1 dt + \int_v^w i_1 dt \\ &= Q_1(t_0 + T) + Q_1(t_0 + 3T/2) \end{aligned}$$

where $u = t_0 + T/2$, $v = t_0 + T$, $w = t_0 + 3T/2$. On the average

$$I_1 = \frac{C_1(V_1 - V_2) + C_2(V_1 - V_2)}{T} \quad (\text{eqn 1.14})$$

$$R = \frac{T}{C_1 + C_2} \quad (\text{eqn 1.15})$$

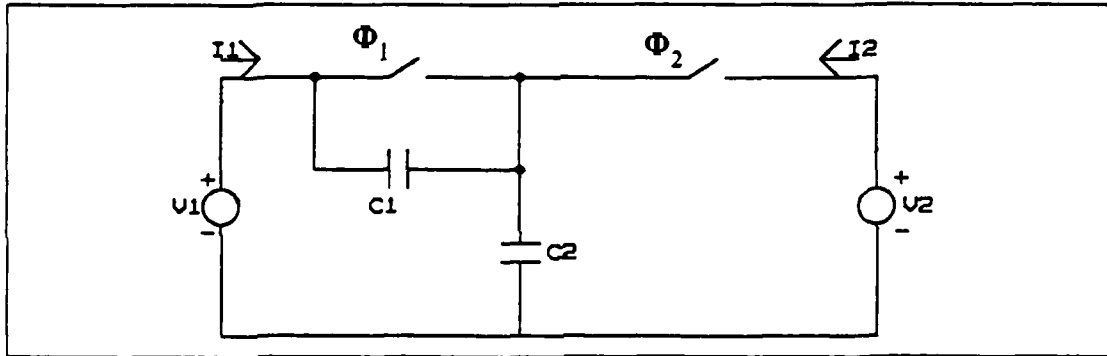


Figure 1.4 The Combination of the Parallel and Series Realization.

This realization is known as series-parallel realization of the continuous resistor. As it was seen from the Equation 1.15 the equivalent resistor depends on C_1 and C_2 . If the capacitor values are chosen equally, then Equation 1.15 becomes

$$R = T/2C \quad (\text{eqn 1.16})$$

Since twice the charge is transferred from one end to another, the resistance value is reduced by 2, as compared to the previous realizations.

There is another realization of the continuous resistor which has indeed the same result as the series-parallel realization. This configuration is shown in Figure 1.5 and known as the bilinear switched capacitance realization of a continuous resistor.

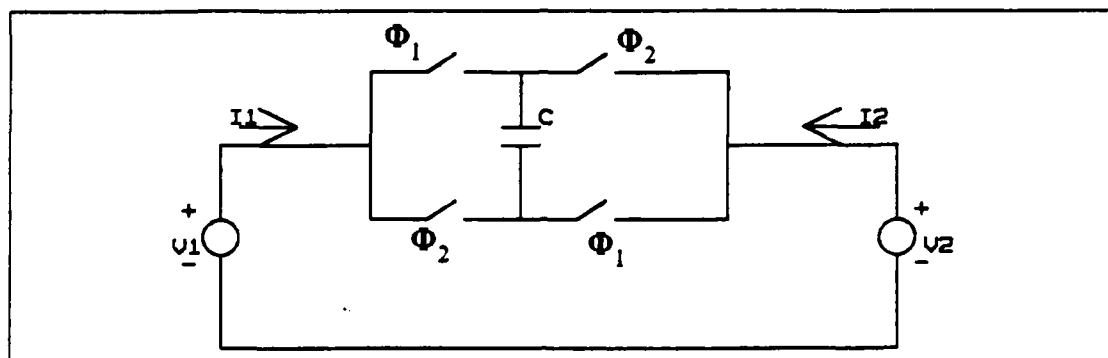


Figure 1.5 The Bilinear SC Realization of a Resistor.

In this approach, all switches change position twice every clock period. Therefore, actual clock period applied to circuit is $T/2$, rather than T . We can put $T/2$ in place of T in Equation 1.16 and obtain

$$R = T/4C \quad (\text{eqn 1.17})$$

In order to show some practical differences of these realizations, some outcomes of the experiments will be discussed and displayed in the next sections.

D. CHARGE CONSERVATION ANALYSIS

This method is a slightly different type of application of Kirchoff's current law, where charge q is used rather than current. In general, because of the two phase clocking operation, a pair of charge equations can be obtained, which characterize the charge conservation condition at a particular node for all sample instants. A pair of charge equations consist of both equations for the even sampling instants and for the odd sampling instants. These are written as follows

for even clock phase (Φ_2)

$$q_1^e(t') = q_m^o(t) + q_c^{o,e}(t), \quad t' > t$$

for odd clock phase (Φ_1)

$$q_1^o(t') = q_m^e(t) + q_c^{o,e}(t), \quad t' > t$$

where $q_i(t')$ is the charge held at one particular node at reference time t' , $q_m(t)$ is the charge at the particular node from the previous phase period, called memory charge, and $q_c(t)$ is the charge injected at that particular node, called contribution charge.

SC networks are characterized mainly in terms of charge-transfer functions on which the discrete-time voltage $v(kT)$ and discrete-time charge differentiation $\Delta q(kT)$ are used as variables.

Assuming a SC network with i capacitors, and N denotes the total number of capacitors connected to a node P during even and odd clock phases, charge variations can be written as

$$\Delta q_p^e(nT) = \sum_i q_{pi}^e(nT) - \sum_i q_{pi}^o[(n-1)T] \quad (\text{eqn 1.18})$$

for even n , and $i = 1, 2, \dots, N_{ep}$.

$$\Delta q_p^o(nT) = \sum_i q_{pi}^o(nT) - \sum_i q_{pi}^e[(n-1)T] \quad (\text{eqn 1.19})$$

for odd n , and $i = 1, 2, \dots, N_{op}$.

In the z -domain, the above charge equations can be described as follows

$$\Delta Q_p^e(z) = \sum_i Q_{pi}^e(z) - z^{-1/2} \sum_i Q_{pi}^o(z) \quad (\text{eqn 1.20})$$

where $i = 1, \dots, N_{ep}$.

$$\Delta Q_p^o(z) = \sum_i Q_{pi}^o(z) - z^{-1/2} \sum_i Q_{pi}^e(z) \quad (\text{eqn 1.21})$$

where $i = 1, \dots, N_{op}$.

Equation 1.18 through Equation 1.21 are going to be used throughout this research.

E. EXPERIMENTAL DEMONSTRATION OF SWITCHED CAPACITOR AS EQUIVALENT RESISTOR

In this section, the mathematical and theoretical relationship between SC networks, of which the output is a sampled analog signal, and the corresponding equivalent resistance value found in the previous section, will be verified experimentally.

As discussed previously, a two phase clock will be needed for all SC network realizations. These two phases can be practically generated from a single clock using a

simple digital circuit shown in Figure 1.6 This circuit is capable of producing two nonoverlapping output clocks that can be used as the two phase clock needed. Output of the NOR gate will be high whenever both inputs are low. This ensures that one phase will be high when the other is low. To provide a larger margin between the two phases of the output clocks (longer nonoverlapping time), two inverters were utilized in each feedback loop to create a longer delay. In the lab, CD4049AE CMOS bipolar gates were used as inverter, which has approximately 15 ns delay time, and CD4001AE CMOS bipolar gates were used as NOR gate, which has 20 ns delay time. Master clock, which is a bipolar square wave, was provided by EXACT MODEL 120 WAVEFORM GENERATOR. The output of the clock circuit is shown in Figures 1.7, 1.8, 1.9. The nonoverlapping time was found to be 50 ns as expected.

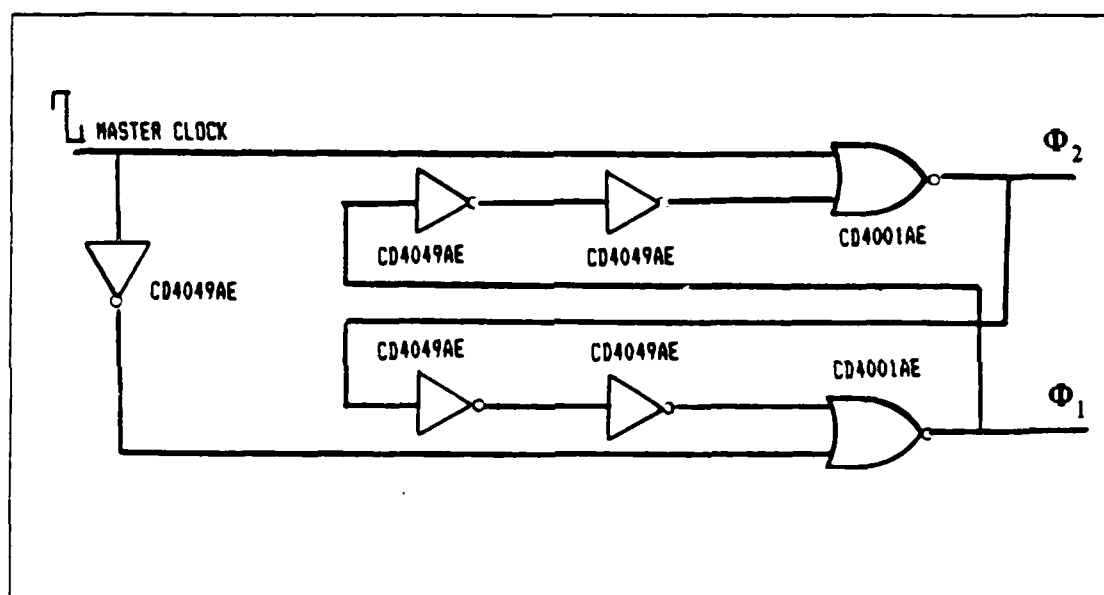


Figure 1.6 The Two Phase Clock Circuit.

Two examples of SC resistor realizations were considered. The first is the parallel switched capacitor realization of a continuous resistance. A simple voltage divider network was constructed using this realization to demonstrate how close the experimental results are to the computed values. This circuit is shown in Figure 1.10. The switches used in this circuit are the CMOS Bilateral Switches CD4066B. These devices are most suitable for switched capacitor applications due to their lower channel resistance (80 ohms maximum), and will be used in all the experiments of this research.

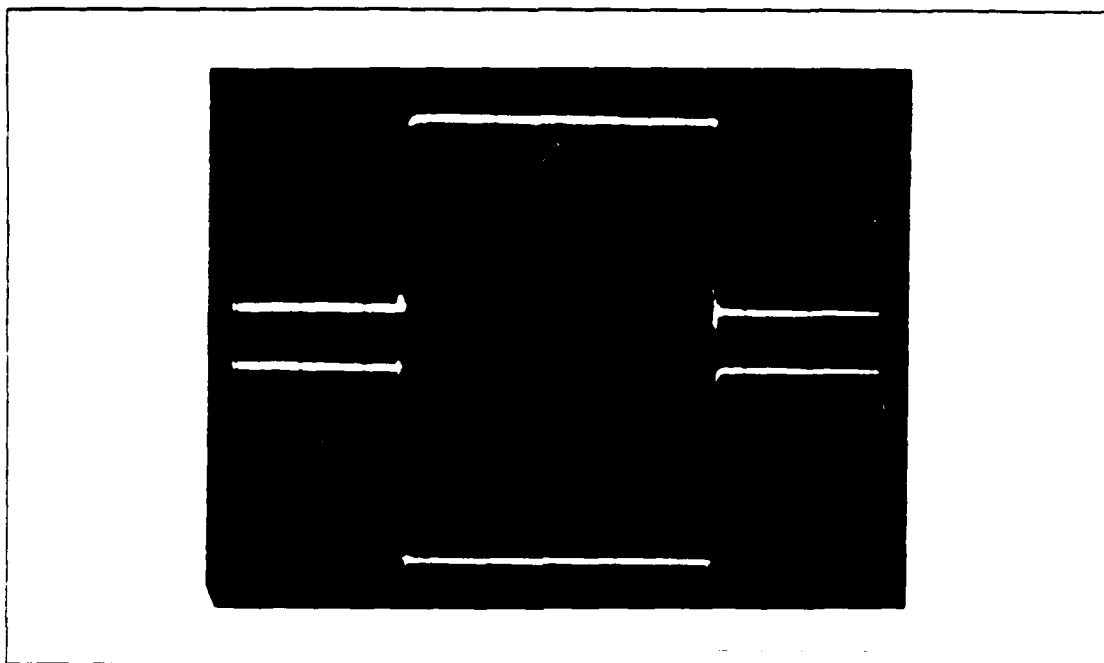


Figure 1.7 Two-Phase Clock.

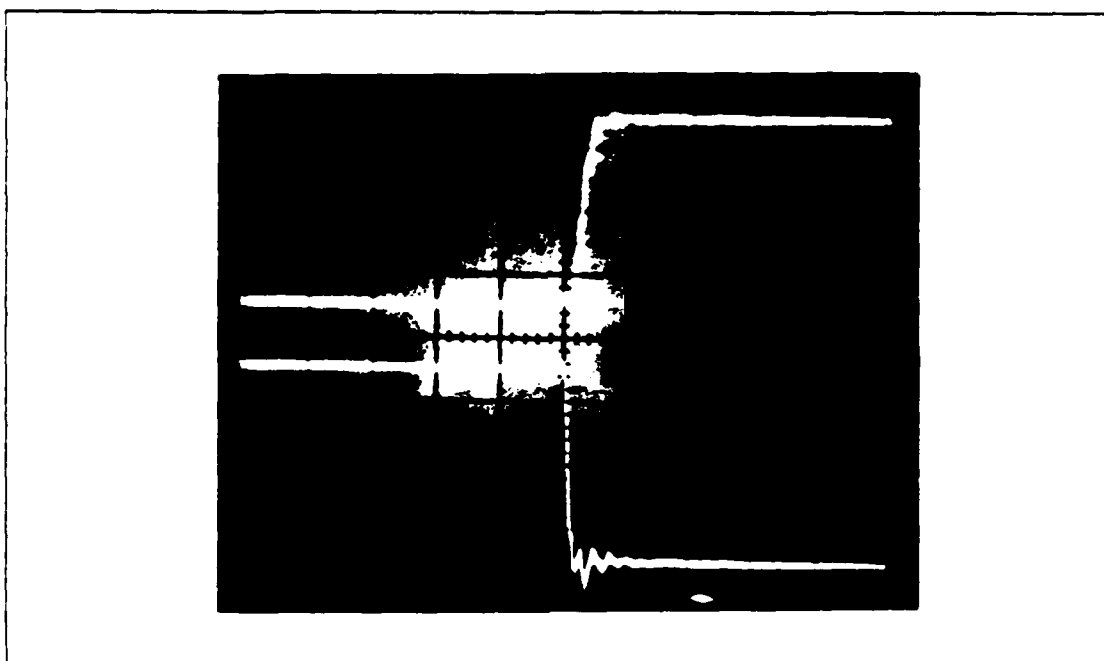


Figure 1.8 Leading Edge.

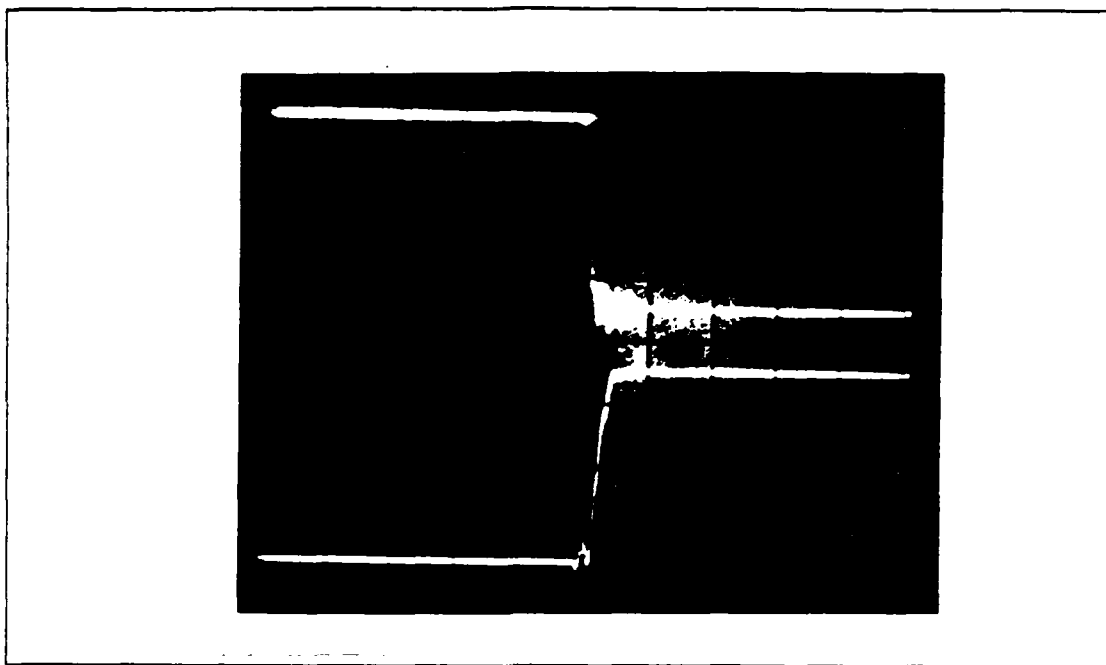


Figure 1.9 Falling Edge.

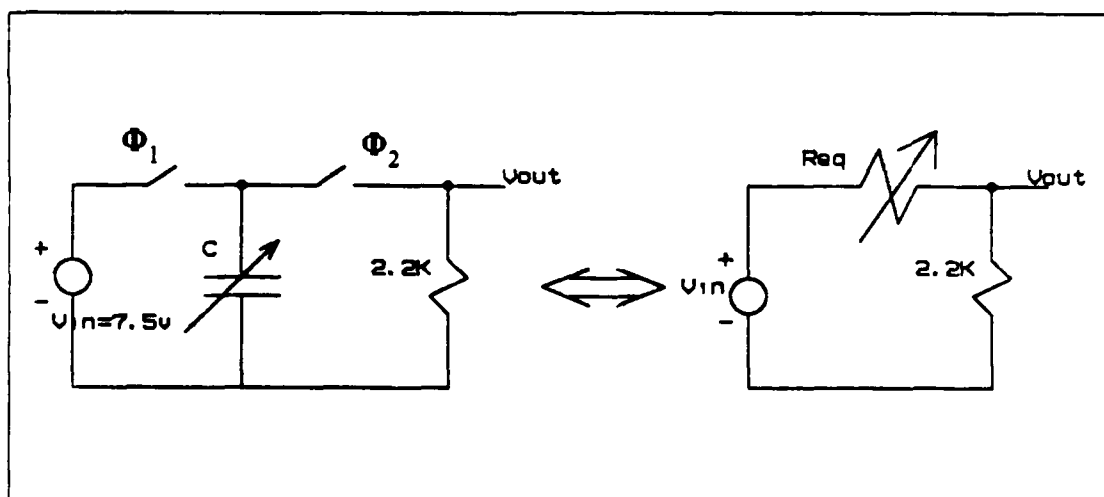


Figure 1.10 Experimental Circuit Using Parallel SC Realization.

The results of this experiment using 50.96 KHz and 101.19 KHz clock frequencies are shown in Figure 1.11 and Figure 1.12.

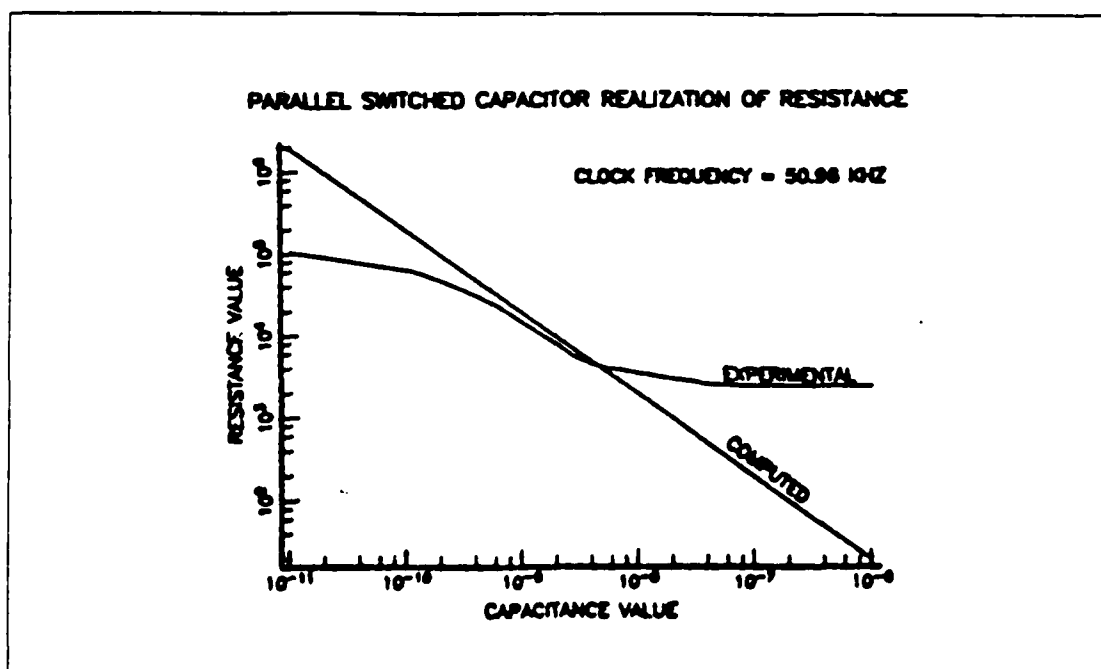


Figure 1.11 Experimental Result of Parallel SC Realization.

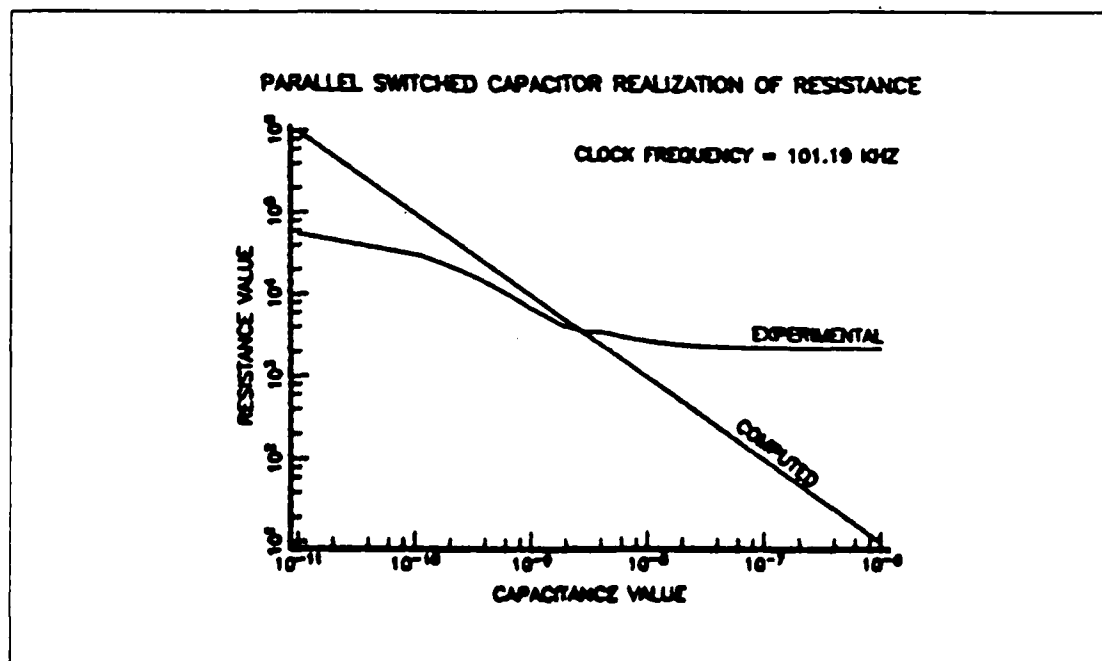


Figure 1.12 Experimental Result of Parallel SC Realization.

The second example is the bilinear switched capacitor realization of a continuous resistance. This experiment was conducted to compare the experimental results obtained using this topology and the theoretical value given by Equation 1.17. The results were also used to show the advantage of this topology over the parallel realization technique. The circuit used in this experiment is shown in Figure 1.13. The result using two different clock frequencies, 51.1 KHz and 101.82 KHz are displayed in Figure 1.14 and Figure 1.15.

In all of the above results, one can notice some deviation between experimental and computed values. These are caused by nonideal properties of the switched capacitor which are going to be discussed later in this section [Ref. 1].

These experimental results show that different SC realizations can be used to simulate resistors when switched capacitor value is within certain range depending on the clock frequency. Otherwise the use of equivalent resistance can lead to gross errors [Ref. 2].

Although the bilinear realization yields a better approximation, there is an important disadvantage which is known as parasitic capacitance. This idea may be shown in Figure 1.16. The parasitic capacitance, C_g , is the capacitance which is virtually placed between one or both plates of the switched capacitor and ground. The value of this parasitic capacitance can reach 10 percent of the switched capacitor [Ref. 3].

Because of this parasitic capacitance, final equivalent resistance value were found to be lower than expected as seen apparently in Figure 1.14 and 1.15. For this reason the value of C can be selected a few percent lower than the nominal value to neglect some of effects of C_g . When C is lower than the computed value, according to Equation 1.17, R becomes larger and matches the computed line in Figure 1.14 and Figure 1.15.

F. NONIDEAL PROPERTIES OF THE SWITCHED CAPACITOR

The use of CMOS FET as switches introduces some secondary effects to the switched capacitor network. These effects may be classified as follows [Ref. 1].

1. Clock feedthrough.
2. Offset error and noise.
3. Nonlinear P-N junction capacitance.
4. Incomplete transfer of charge.

These secondary effects will be studied throughout this research.

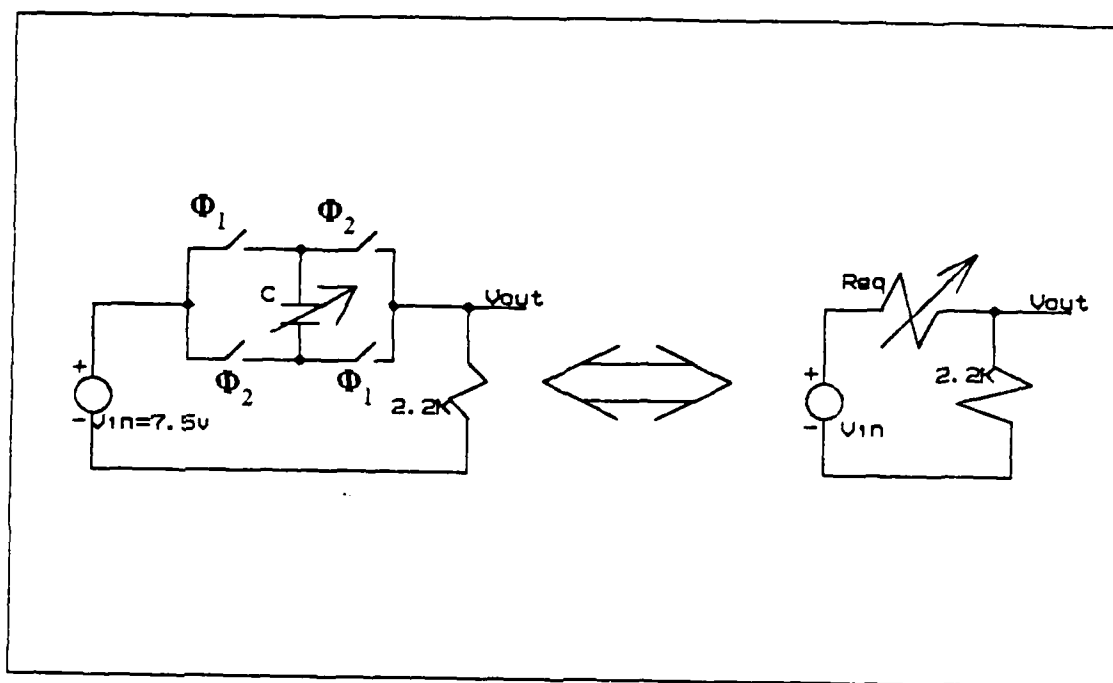


Figure 1.13 Experimental Circuit Using Bilinear SC Realization.

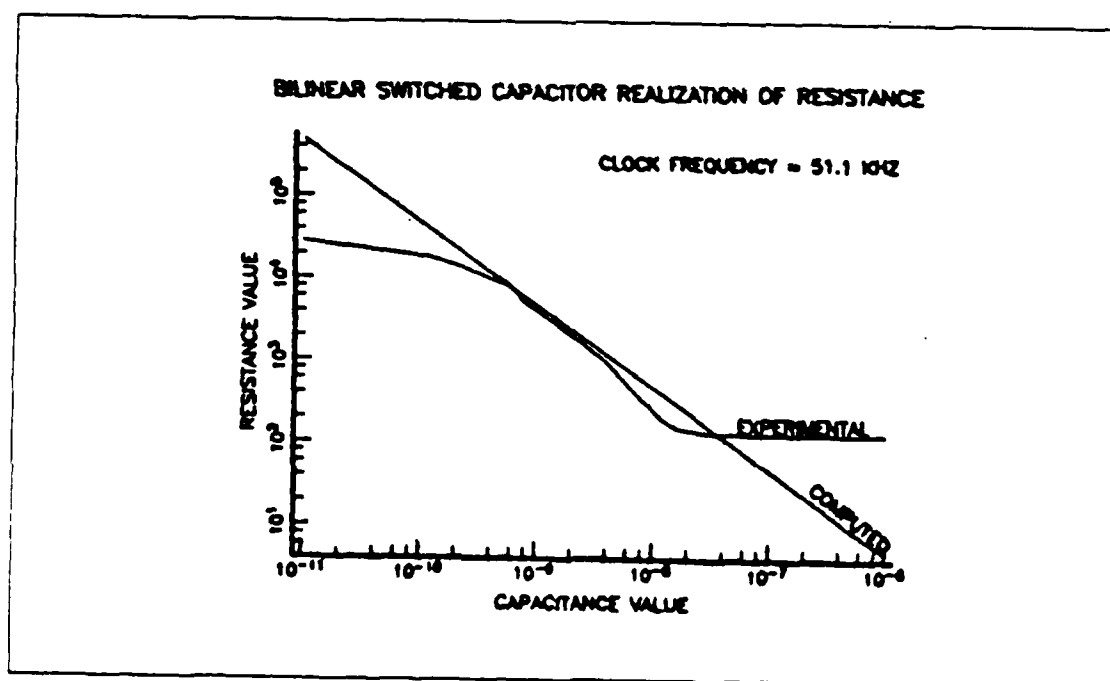


Figure 1.14 Experimental Result of Bilinear SC Realization.

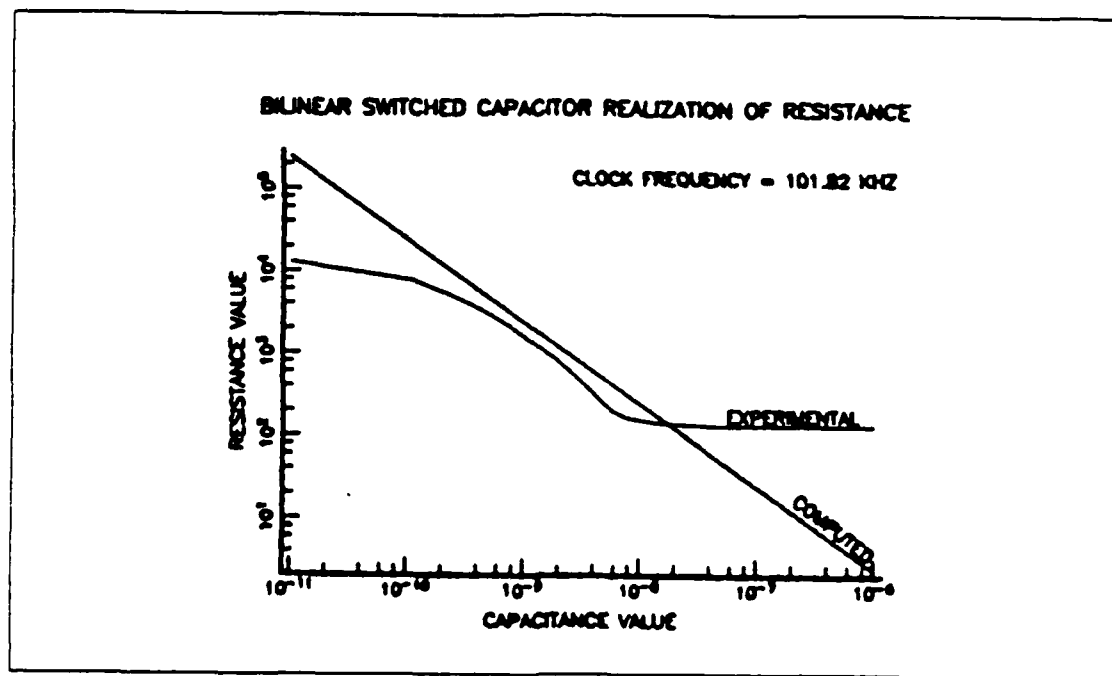


Figure 1.15 Experimental Result of Bilinear SC Realization.

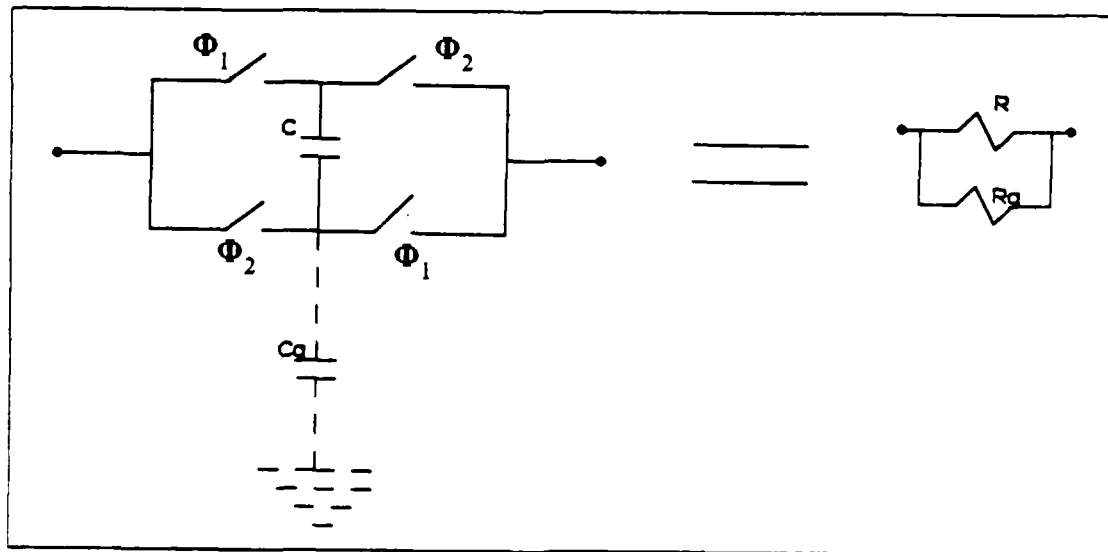


Figure 1.16 Appearing of the Parasitic Capacitance.

II. THE BILINEAR TRANSFORMATION AS A SC FILTER DESIGN TECHNIQUE

A. GENERAL

Since the switched capacitor filters are sampled version of analog filters, the main goal of this chapter is to set up a bridge between continuous and discrete time domains, and use this as a design tool.

Since filters are typically specified by frequency-domain requirements, it is convenient to have a mathematical expression that allows to transform rational s-domain transfer functions to rational z-domain transfer functions. Such an expression should possess two qualities:

1. Stable s-domain transfer functions map into stable z-domain transfer functions.
2. The imaginary $j\omega$ -axis of the s-plane map onto the unit circle of z-plane.

Item 1 ensures that transformed z-domain transfer functions will be stable. Item 2 ensures that not only will they be stable but that the shape of the gain response can be preserved.

From digital signal processing environment, there are several major mapping procedures which are used to transfer the information from s-domain into the z-domain or vice versa. They are as follows

1. Backward Difference (BD) Transformation
2. Forward Difference (FD) Transformation
3. Lossless Discrete Integrator (LDI) Transformation
4. Bilinear Transformation

By setting $s = -\alpha + j\omega$ and evaluating z , it can be determined whether items 1 and 2 are satisfied. The backward difference transformation maps the $j\omega$ -axis inside the unit circle. Thus, item 1 is satisfied; however, item 2 is not. This mapping is stated as follows

$$z = 1 / (1 - sT) \quad (\text{eqn 2.1})$$

Applying the same procedure for the forward difference transformation, it can be showed that the FD maps the $j\omega$ -axis into a straight line outside the unit circle. Thus, the forward difference transformation satisfied neither item 1 nor 2. This transformation can be expressed as follows

$$z = 1 + sT \quad (\text{eqn 2.2})$$

It can be concluded that the forward difference transformation maps s-plane poles and zeros with high quality factor into z-plane poles and zeros with higher quality factor. The resulting z-plane poles may be unstable. One can determine that the FD is unsuitable and that the BD is marginally suitable (for $\omega T \ll 1$) for transformation.

The lossless discrete integrator (LDI) transformation and the bilinear transformation satisfy two qualities. But, the LDI transformed transfer functions being realized require twice as much hardware as that required to realize bilinear transformed transfer functions. In the previous chapter, the results of the experiments showed that the bilinear realization of the continuous resistance would appear better than others. The bilinear realization is also very related to the bilinear mapping procedure that will be explained later in this chapter (Section E). For these reasons, the bilinear transformation will be deeply studied and vital points underlined so that one can use these points as a design aids.

B. BILINEAR TRANSFORMATION

The bilinear transformation is a method which is based on numerical analysis techniques. It solves the difference equation, which represents the system, according to the trapezoidal rule. In order to illustrate the technique let us follow an example. As a notation, $x_a(t)$ is used for input signal of an analog system and $y_a(t)$ as the output signal of the system. Let us assume that these two signals are related to each other by the first-order differential equation

$$b_1 \frac{dy_a(t)}{dt} + b_0 y_a(t) = a_0 x(t) \quad (\text{eqn 2.3})$$

The corresponding analog system transfer function is

$$H(s) = \frac{a_0}{b_1 s + b_0} \quad (\text{eqn 2.4})$$

$y_a(t)$ can be expressed as follows

$$y_a(t) = \int_{t_0}^t \frac{dy_a(\tau)}{d\tau} d\tau + y_a(t_0) \quad (\text{eqn 2.5})$$

In this step, if the signal is sampled every T second and if $t = nT$, $t_0 = (n-1)T$, then

$$y_a(nT) = \int_{(n-1)T}^{nT} y'_a(\tau) d\tau + y_a((n-1)T) \quad (\text{eqn 2.6})$$

If the integral process is evaluated by the trapezoidal rule we obtain

$$y_a(nT) = y_a((n-1)T) + T [y'_a(nT) + y'_a((n-1)T)] \quad (\text{eqn 2.7})$$

From the original differential equation

$$y'_a(nT) = -\frac{b_0}{b_1} y_a(nT) + \frac{a_0}{b_1} x_a(nT)$$

substituting into Equation 2.7 we obtain

$$y_a(nT) - y_a((n-1)T) = T \left[-\frac{b_0}{b_1} (y_a(nT) + y_a((n-1)T)) + \frac{a_0}{b_1} (x_a(nT) + x_a((n-1)T)) \right]$$

Taking the z-transform and solving for $H(z)$ gives

$$H(z) = \frac{Y(z)}{X(z)} = \frac{a_0}{b_1 \frac{2}{T} \frac{1-z^{-1}}{1+z^{-1}} + b_0} \quad (\text{eqn 2.8})$$

If $H(z)$ is compared with $H(s)$, relationship between s and z can be obtained easily and written

$$H(z) = H(s) \Big|_{s = \left(\frac{2}{T} \frac{1-z^{-1}}{1+z^{-1}} \right)} \quad (\text{eqn 2.9})$$

This can be shown to hold in general since an N^{th} -order differential equation can be written as a set of N first-order equations of the form of Equation 2.3.

$$s = \frac{2}{T} \frac{1-z^{-1}}{1+z^{-1}} \quad (\text{eqn 2.10})$$

or

$$z = \frac{1 + (T/2)s}{1 - (T/2)s} \quad (\text{eqn 2.11})$$

That is, the invertible transformation of Equation 2.10 is recognized as a bilinear transformation. Setting $s = \alpha + j\omega$ give us

$$z = \frac{1 + (T/2)(\alpha + j\omega)}{1 - (T/2)(\alpha + j\omega)} \quad (\text{eqn 2.12})$$

by letting $z = re^{j\theta}$, we obtain

$$r = \frac{\sqrt{((2/T) + \alpha)^2 + \omega^2}}{\sqrt{((2/T) - \alpha)^2 + \omega^2}} \quad \text{and}$$

$$\theta = \tan^{-1}\left(\frac{\omega}{2/T + \alpha}\right) - \tan^{-1}\left(\frac{\omega}{2/T - \alpha}\right) \quad (\text{eqn 2.13})$$

From Equation 2.13 the bilinear transformation maps

1. The right-half of the s -plane onto the region exterior to the unit circle where $|z| = 1$ of the z -plane. This comes from the fact that $\alpha > 0$, $r > 1$.
2. The imaginary axis of the s -plane onto the unit circle, $|z| = 1$, of the z -plane. This comes from the fact that $\alpha = 0$, $z = \exp[j2\tan^{-1}(\omega T/2)]$.
3. The left-half of the s -plane onto the interior of the unit circle, $|z| = 1$, of the z -plane, because for $\alpha < 0$, $r < 1$.

From item 2 several other important observations can be made. For $\alpha = 0$ and $\omega = 0$, $z = 1e^{j0}$ which indicate that the s -plane origin maps to the point (1,0) in the z -plane. For $\alpha = 0$ and $\omega \rightarrow \infty$, $z = 1e^{j\pi}$ and for $\alpha = 0$ and $\omega \rightarrow -\infty$, $z = 1e^{-j\pi}$ which indicate that the positive and negative ω -axis in the s -plane map onto the upper and lower semi-circles where $|z| = 1$ in the z -plane. Obviously, a stable analog filter produces a stable digital filter.

Since the entire imaginary axis ($s = j\omega$) in the s -plane, maps onto the unit circle ($|z| = 1$) in the z -plane, nonlinear relationship between analog and digital frequencies can be easily seen. The distortion introduced here is known as the warping effect and it is illustrated using Equation 2.10 for $s = j\omega$ and $z = e^{j\theta}$.

$$\begin{aligned}
jw &= \frac{2 e^{j\theta} - 1}{T e^{j\theta} + 1} \\
&= \frac{2 e^{j\theta/2} (e^{j\theta/2} - e^{-j\theta/2})}{T e^{j\theta/2} (e^{j\theta/2} + e^{-j\theta/2})} \\
jw &= \frac{2}{T} j \frac{\sin(\theta/2)}{\cos(\theta/2)}
\end{aligned} \tag{eqn 2.14}$$

and thus the imaginary axis in the s-plane is related to the unit circle in the z-plane through the relation

$$w = (2/T) \tan(\theta/2) \tag{eqn 2.15}$$

where θ is the digital frequency and w is the analog frequency.

To obtain $H(z)$ from $H(s)$ is rather tedious and time consuming. This transformation thus is generally done by the computer. For a second-order transfer function a computer program has been written and presented in Appendix A.

C. THE EFFECTS OF HIGH SAMPLING RATE

In the mapping process, generally the s-domain specifications of the filter are known. But, there might be some ambiguity if it is the case of obtaining a function $H(s)$ from a given function $H(z)$. However, when the sampling rate is much greater than the frequencies of interest, various assumptions can be made to obtain approximate relationships between the two domains.

For small $|s|T$, Equation 2.11 can be written

$$z = 1 + sT + \frac{(sT)^2}{2} + \frac{(sT)^3}{4} + \dots \tag{eqn 2.16}$$

For high sampling rates, the second-order effects can be ignored, so Equation 2.11 can be approximated as

$$z = 1 + sT \tag{eqn 2.17}$$

Equation 2.17 shows that as the sampling period T is decreased, or sampling frequency increased, z approaches the point $z = 1$.

The characteristic equation of the second-order analog filter can be expressed as

$$s^2 + \frac{W_n}{Q}s + W_n^2 = 0 \quad \text{where } Q \text{ is the quality factor} \quad (\text{eqn 2.18})$$

The solution of the characteristic equation, that is the poles of the system can be described as

$$s_{1,2} = -\frac{W_n}{2Q} \pm j\frac{W_n}{2Q}\sqrt{4Q^2 - 1} \quad (\text{eqn 2.19})$$

On the other hand, the characteristic equation of the second-order digital filter can be written as follows

$$z^2 - 2r\cos\theta z + r^2 = 0 \quad (\text{eqn 2.20})$$

using the approximation obtained in Equation 2.17

$$z_{1,2} = 1 + s_{1,2}T \quad \text{consequently}$$

$$z_{1,2} = re^{\pm j\theta}$$

$$r = \sqrt{1 - (W_n T/Q) + (W_n T)^2} \quad (\text{eqn 2.21})$$

$$\theta = \tan^{-1} \frac{W_n T \sqrt{4Q^2 - 1}}{2Q - W_n T} \quad (\text{eqn 2.22})$$

if Equation 2.21 is solved for Q

$$Q = \frac{W_n T}{(1-r)(1+r) + (W_n T)^2} \quad (\text{eqn 2.23})$$

if Q is greater than unity as well as assuming high sampling rate, Equation 2.23 can be approximated as

$$Q \sim \frac{W_n T}{2(1-r) + (W_n T)^2} \quad (\text{eqn 2.24})$$

In the case of high sampling rate warping effect can be neglected and $\theta \sim W_n T$. Thus Equation 2.24 becomes

$$Q \sim \frac{\theta}{2(1-r)} \quad \text{for } 2(1-r) \gg (W_n T)^2 \quad (\text{eqn 2.25})$$

from Equation 2.25, r can be approximated as

$$r \cong 1 - \frac{\theta}{2Q} \quad (\text{eqn 2.26})$$

and $\cos\theta$ can be written as

$$\cos\theta \cong 1 - \frac{\theta^2}{2} \quad (\text{eqn 2.27})$$

Note that Equation 2.21 through Equation 2.27 are valid at high sampling rates and for large value of Q . For simplicity, if the characteristic equation of the z -domain transfer function is considered as

$$z^2 + b_1 z + b_2 = 0$$

$$W_n = K \frac{\sqrt{1+b_1+b_2}}{\sqrt{1-b_1+b_2}} \quad (\text{eqn 2.28})$$

For bilinear transformation,

$$Q = \frac{\sqrt{(1+b_1+b_2)(1-b_1+b_2)}}{2(1-b_2)} \quad (\text{eqn 2.29})$$

where K is a constant involving a frequency prewarping [Ref. 4] and is given by

$$K = \frac{W}{\tan(\theta/2)} \quad (\text{eqn 2.30})$$

When high sampling rate condition is satisfied, $\theta/2 \ll 1$, K simply becomes

$$K = 2/T \quad (\text{eqn 2.31})$$

D. ELEMENT TRANSFORMATIONS

In order to treat SC filters in z-domain, some concepts which don't exist in digital filters should be considered. These concepts are basically associated with passive circuit elements, which are inductances, capacitances and resistances.

If the bilinear transformation is used directly to obtain the admittances, one can use the results as an equivalent elements which are derived as follows. This method is usually known as Building Block Approach.

1. Capacitor

If the relationship between current and voltage across a capacitor is written as

$$i(t) = c \frac{dv(t)}{dt} \quad \text{that is,} \quad \frac{dq(t)}{dt} = c \frac{dv(t)}{dt}$$

by taking Laplace transform of both sides

$$sQ(s) - q(0) = c[sV(s) - V(0)] \quad \text{where, } \mathcal{L}[q(t)] = Q(s) \text{ and } \mathcal{L}[v(t)] = V(s).$$

$q(0) = v(0) = 0$ as initial conditions.

$$Q(s)V(s) = C$$

using bilinear transformation

$$Y_c = \frac{Q(z)}{V(z)} = C \quad (\text{eqn 2.32})$$

Equation 2.32 can be considered as admittance, which is not the way it is described. This new definition comes from the fact that the analysis of the SC circuit is done by using charge variation equations.

2. Resistor

If the same procedure followed for capacitor is applied for resistor, the following equations can be easily written.

Since $i(t) = Gv(t)$ where $G = 1/R$

$$\frac{dq(t)}{dt} = Gv(t)$$

taking Laplace transform of both sides

$$sQ(s) - q(0) = GV(s) \quad \text{where } q(0) = 0$$

$$\frac{Q(s)}{V(s)} = \frac{G}{s}$$

using bilinear transform yields

$$Y_R = \frac{Q(z)}{V(z)} = \frac{G}{s} = \frac{GT}{2} \frac{1+z^{-1}}{1-z^{-1}} \quad (\text{eqn 2.33})$$

3. Inductor

The instantaneous voltage and current for an inductor L are related by

$$v(t) = L \frac{di(t)}{dt}$$

$$v(t) = L \frac{d^2q(t)}{dt^2}$$

taking Laplace transform

$$V(s) = L[s^2Q(s) - sq(0) - q'(0)] \quad \text{where } q(0) = q'(0) = 0$$

$$\frac{Q(s)}{V(s)} = \frac{1}{Ls^2} \quad \text{using bilinear transformation yields}$$

$$Y_L = \frac{Q(z)}{V(z)} = \frac{1}{Ls^2} = \frac{T^2}{4L} \frac{(1+z^{-1})^2}{(1-z^{-1})^2} \quad (\text{eqn 2.34})$$

To express the single floating capacitor shown in Figure 2.1, charge variation equations, Equation 1.20 and Equation 1.21, can be used.

$$\Delta Q_1^e(z) = CV_1^e(z) - Cz^{-1/2}V_1^o(z) - CV_2^e(z) + Cz^{-1/2}V_2^o(z)$$

$$\Delta Q_1^o(z) = CV_1^o(z) - Cz^{-1/2}V_1^e(z) - CV_2^o(z) + Cz^{-1/2}V_2^e(z)$$

$$\Delta Q_2^e(z) = CV_2^e(z) - Cz^{-1/2}V_2^o(z) - CV_1^e(z) + Cz^{-1/2}V_1^o(z)$$

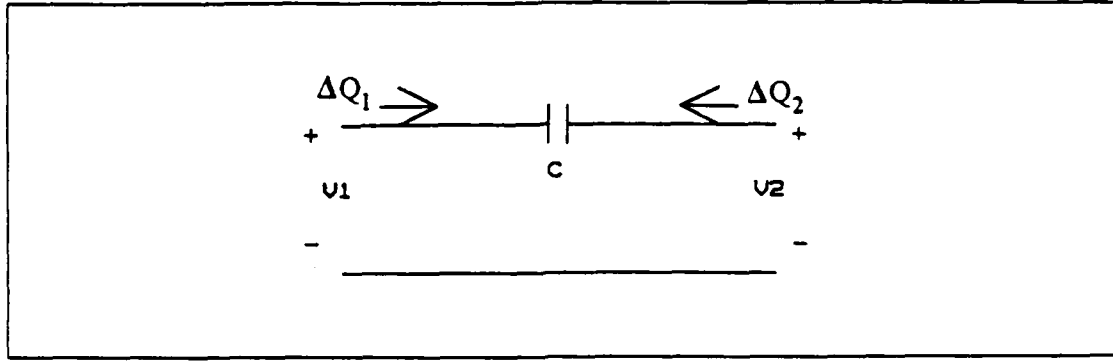


Figure 2.1 Floating Capacitor.

$$\Delta Q_2^o(z) = CV_2^o(z) - Cz^{-1/2}V_2^e(z) - CV_1^o(z) + Cz^{-1/2}V_1^e(z)$$

From these equations

$$\begin{aligned} \Delta Q_1^e(z) + \Delta Q_1^o(z) &= C(1 - z^{-1/2})[V_1^e(z) + V_1^o(z)] \\ &\quad - C(1 - z^{-1/2})[V_2^e(z) + V_2^o(z)] \end{aligned} \quad (\text{eqn 2.35})$$

and

$$\begin{aligned} \Delta Q_2^e(z) + \Delta Q_2^o(z) &= C(1 - z^{-1/2})[V_2^e(z) + V_2^o(z)] \\ &\quad - C(1 - z^{-1/2})[V_1^e(z) + V_1^o(z)] \end{aligned} \quad (\text{eqn 2.36})$$

Since $\Delta Q(z) = \Delta Q^e(z) + \Delta Q^o(z)$ and

$$V(z) = V^e(z) + V^o(z)$$

Equation 2.35 and Equation 2.36 can be written as

$$\Delta Q_1(z) = C(1 - z^{-1/2})V_1(z) - C(1 - z^{-1/2})V_2(z) \quad (\text{eqn 2.37})$$

$$\Delta Q_2(z) = C(1 - z^{-1/2})V_2(z) - C(1 - z^{-1/2})V_1(z) \quad (\text{eqn 2.38})$$

From Equation 2.37 and 2.38, admittance Y_c appears as $Y_c = C(1 - z^{-1/2})$

Since $z^{-1} = e^{-j\omega T}$ then $z^{-1/2} = e^{-j\omega T/2}$, even though the period of the sampling decreases to half of the original value. Then

$$(z')^{-1} = z^{-1/2} \text{ can be written.}$$

$$Y_c = C(1 - (z')^{-1}) \quad (\text{eqn 2.39})$$

Since Equation 2.39 is realizable with simple SC networks, we can compare this, Y_c , with Equation 2.32 and consider $(1 - (z')^{-1})$ factor as a scaling factor [Ref. 5]. Therefore Equation 2.32, Equation 2.33, and Equation 2.34 can be written as

$$Y_c = C(1 - z^{-1}) \quad (\text{eqn 2.40})$$

$$Y_R = GT/2(1 + z^{-1}) \quad (\text{eqn 2.41})$$

$$Y_L = \frac{T^2 (1 + z^{-1})^2}{4L (1 - z^{-1})} \quad (\text{eqn 2.42})$$

This would be a good place to revisit the bilinear switched capacitance realization of the continuous resistor shown in Figure 1.5. It is also known as the floating bilinear resistor. Charge equations in z-domain are

$$\begin{aligned} \Delta Q^e_1(z) &= CV^e_1(z) + Cz^{-1/2}V^o_1(z) - CV^e_2(z) - Cz^{-1/2}V^o_2(z) \\ \Delta Q^o_1(z) &= CV^o_1(z) + Cz^{-1/2}V^e_1(z) - CV^o_2(z) - Cz^{-1/2}V^e_2(z) \\ \Delta Q^e_2(z) &= CV^e_2(z) + Cz^{-1/2}V^o_2(z) - CV^e_1(z) - Cz^{-1/2}V^o_1(z) \\ \Delta Q^o_2(z) &= CV^o_2(z) + Cz^{-1/2}V^e_2(z) - CV^o_1(z) - Cz^{-1/2}V^e_1(z) \end{aligned}$$

$$\Delta Q^e_1(z) + \Delta Q^o_1 = C(1 + z^{-1/2})V_1(z) - C(1 + z^{-1/2})V_2(z) \quad (\text{eqn 2.43})$$

$$\Delta Q^e_2(z) + \Delta Q^o_2(z) = C(1 + z^{-1/2})V_2(z) - C(1 + z^{-1/2})V_1(z) \quad (\text{eqn 2.44})$$

Equation 2.43 and Equation 2.44 yields

$$Y_R = C(1 + z^{-1/2}) \quad (\text{eqn 2.45})$$

Since $(z')^{-1} = z^{-1/2}$, this can be written as

$$Y_R = C(1+(z')^{-1}) \quad (\text{eqn 2.46})$$

if Equation 2.46 is compared to Equation 2.41

$$Y_R = (GT'/2)(1+(z')^{-1}) = C(1+(z')^{-1})$$

$$G = 2C/T$$

$$R = \frac{T'}{2C} \quad \text{and} \quad T' = T/2$$

$$R = \frac{T}{4C} \quad (\text{eqn 2.47})$$

which is the same as Equation 1.17, as expected.

E. INTEGRATORS USING BILINEAR TRANSFORMATION

Since the integrators are widely used circuits in analog signal processing, their transfer functions will be investigated and compared with the results obtained in the lab to decide how much error would be introduced using bilinear transformation.

1. Lossless Integrator

An analog lossless integrator is shown in Figure 2.2. If the resistor is replaced by the bilinear SC resistor equivalent circuits presented in Chapter I, Figure 2.3 is obtained and obviously

$$C_1 = \frac{T}{4R_1}$$

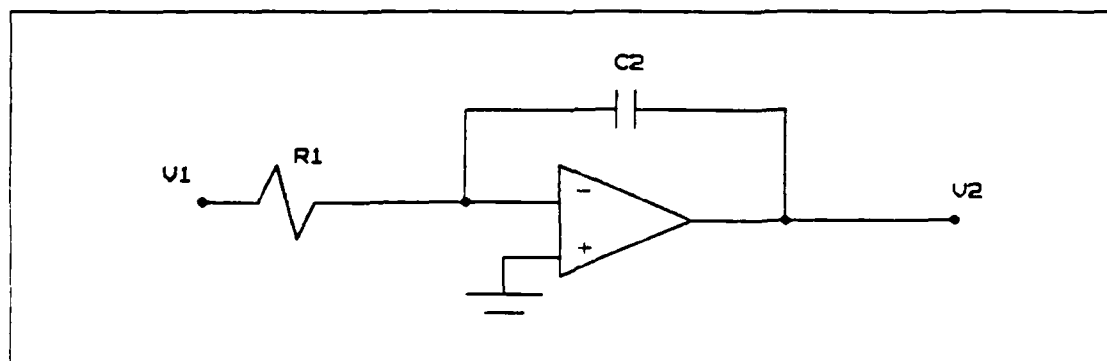


Figure 2.2 An Analog Integrator.

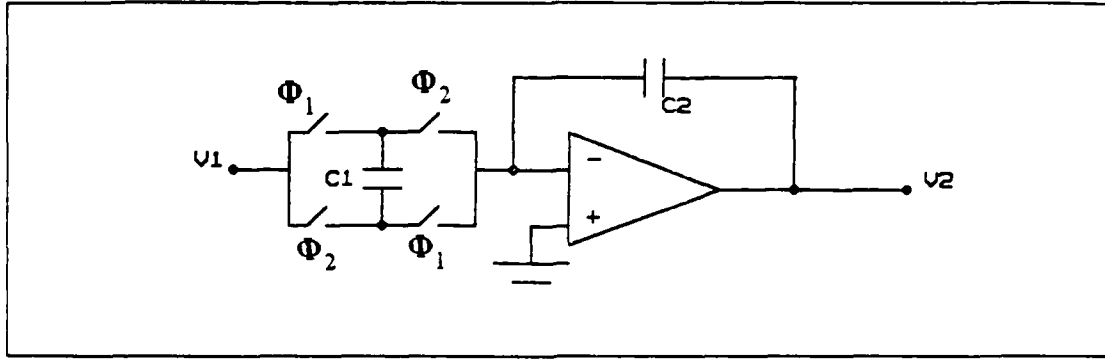


Figure 2.3 Bilinear SC Integrator.

if charge variation equations are written in the z-domain,

$$C_2 V_2^o(z) = C_2 V_2^e(z) z^{-1/2} - C_1 V_1^e(z) z^{-1/2} - C_1 V_1^o(z) \quad (\text{eqn 2.48})$$

can be obtained for odd phase and

$$C_2 V_2^e(z) = C_2 V_2^o(z) z^{-1/2} - C_1 V_1^o(z) z^{-1/2} - C_1 V_1^e(z) \quad (\text{eqn 2.49})$$

can be obtained for even phase. Knowing that

$$V_1(z) = V_1^e(z) + V_1^o(z)$$

$$V_2(z) = V_2^e(z) + V_2^o(z)$$

from Equation 2.48 and Equation 2.49

$$H(z) = \frac{V_2(z)}{V_1(z)} = -\frac{C_1}{C_2} \frac{(1 + z^{-1/2})}{(1 - z^{-1/2})} \quad (\text{eqn 2.50})$$

Since $z^{-1/2} = (z')^{-1}$ the transfer function $H(z)$ is rewritten as

$$H(z') = -\frac{C_1}{C_2} \left(\frac{1 + (z')^{-1}}{1 - (z')^{-1}} \right) \quad (\text{eqn 2.51})$$

Transfer function for a simple analog integrator is

$$H(s) = -\frac{1}{R_1 C_2 S} \quad \text{where} \quad R_1 = \frac{T}{2C_1}, \quad \text{as in Equation 1.16}$$

$$H(s) = - \frac{2C_1}{C_2TS} \quad (\text{eqn 2.52})$$

If Equation 2.51 is compared to Equation 2.52

$$s = \frac{2}{T} \left(\frac{1-z^{-1}}{1+z^{-1}} \right)$$

which is nothing more than bilinear mapping.

The lossless integrator would not be implemented due to the fact that the operational amplifier requires some dc feedback. The computer simulations of both $H(s)$ and $H(z)$ are shown in Figure 2.4 and Figure 2.5. These figures demonstrate clearly the nonlinear relationship between s-domain and z-domain due to the warping property introduced by the bilinear transformation.

2. Lossy Integrator and Experimental Results

As mentioned earlier, the lossless integrator can not be realized in practice. Instead, the lossy integrator is considered in practical SC circuit. The lossy bilinear integrator is shown in Figure 2.6. The analog lossy integrator's transfer function $H(s)$ can be written as

$$H(s) = \frac{V_o(s)}{V_i(s)} = - \frac{1}{R_1 C_2 (s + 1/(R_3 C_2))} \quad (\text{eqn 2.53})$$

where $R_1 = T/(4C_1)$ and $R_3 = T/(4C_3)$.

If a high sampling rate is used the warping effect can be ignored. The bilinear transformation yields the following

$$H(z') = -2 \frac{C_1}{C_3} \frac{(1+(z')^{-1})}{2(1+(z')^{-1}) + C_2/C_3(1-(z')^{-1})} \quad (\text{eqn 2.54})$$

As an experimental set of values in the lab,

$$C_1 = 226 \text{ pf}$$

$$C_2 = 431 \text{ pf}$$

$$C_3 = 4.2 \text{ pf}$$

were chosen and CD4066 CMOS switches and LM741 Operational Amplifiers were used. $H(z')$ was obtained by the computer program given in Appendix A, using the following equation.

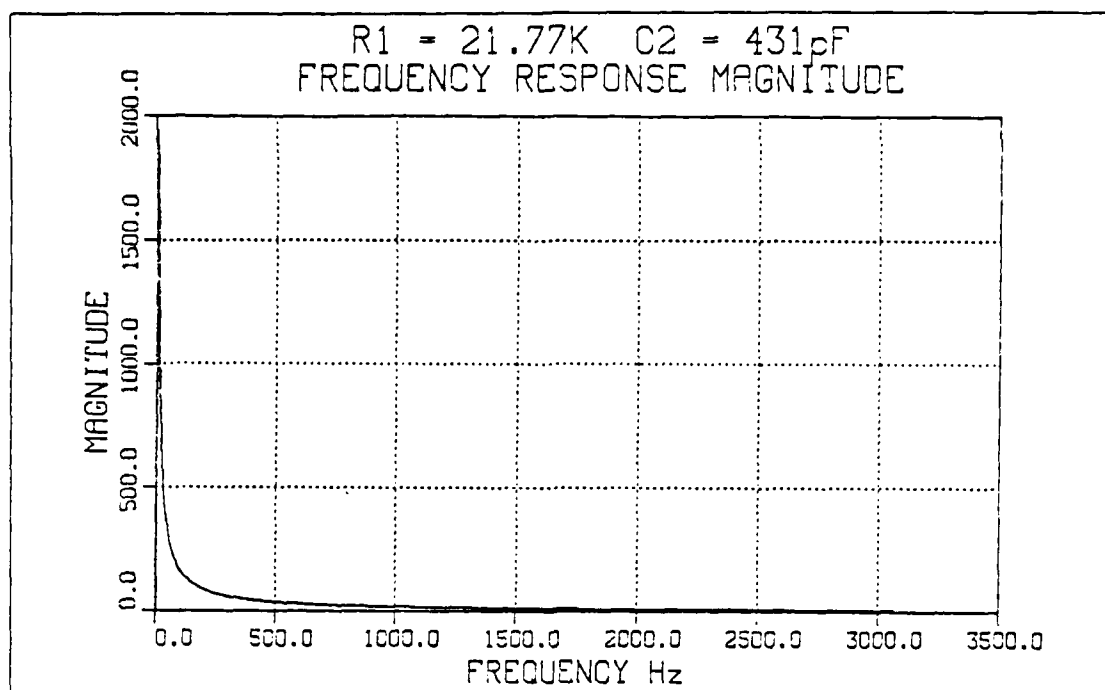


Figure 2.4 Bode Plot for an Analog Integrator.

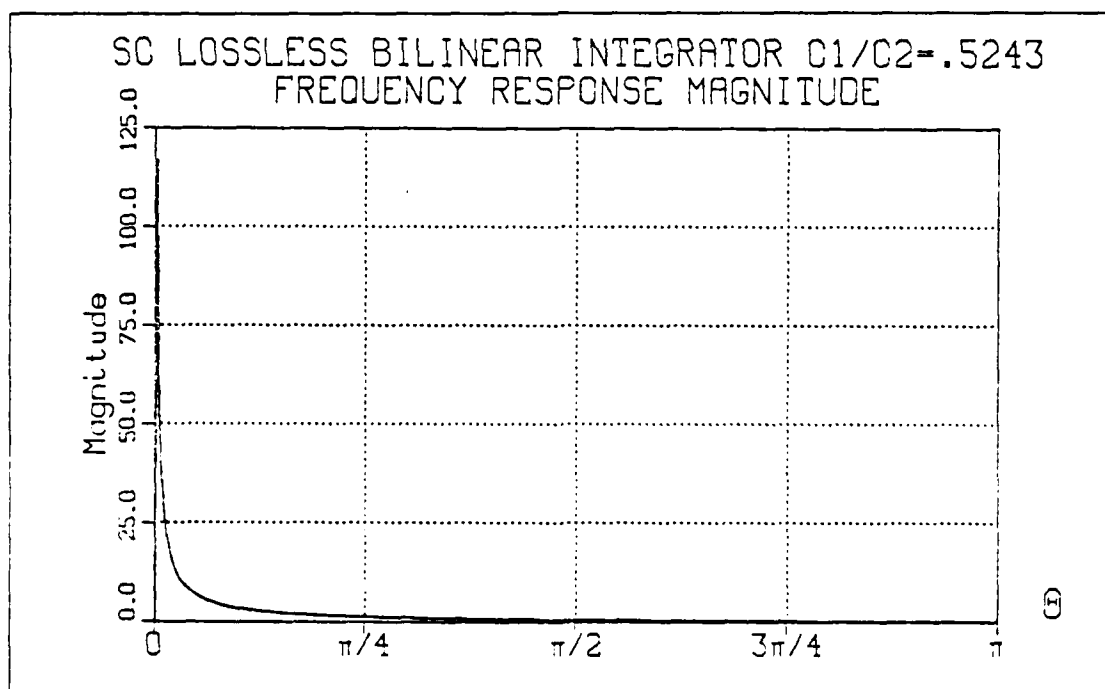


Figure 2.5 Magnitude Response for the Bilinear SC Integrator.

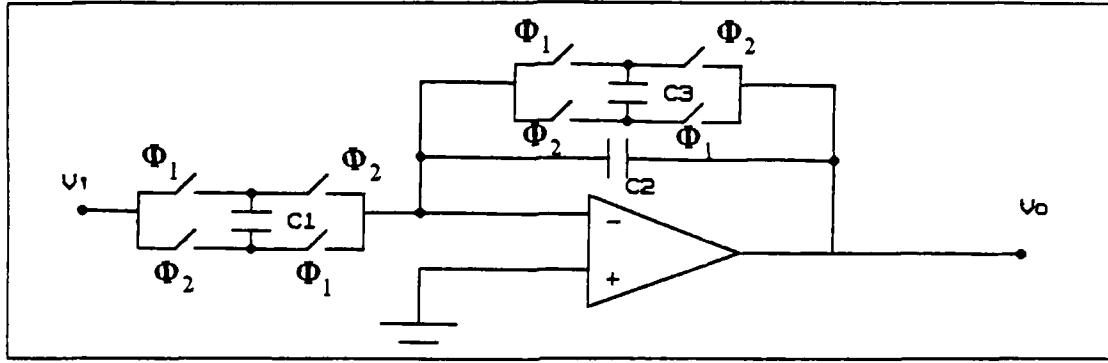


Figure 2.6 The Lossy Bilinear Integrator.

$$H(s) = -1.066 \cdot 10^5 \frac{1}{s + 1.9841 \cdot 10^3} \quad (\text{eqn 2.55})$$

$$H(z') = - \frac{0.5195(z')^2 + 1.039z' + 0.5195}{(z')^2 + 0.0193z' - 0.98066} \quad \text{with } f_c = 50.8 \text{ KHz} \quad (\text{eqn 2.56})$$

The computer simulation results were displayed in Figure 2.7, Figure 2.8, Figure 2.9, and Figure 2.10. Using building block approach, the transfer function of Figure 2.6 can be readily written as follows

$$H(z') = - \frac{C_1}{C_2} \frac{(1 + (z')^{-1})}{(1 + C_3/C_2) - (1 - (C_3/C_2)z')}$$

(eqn 2.57)

Using the previous capacitor values $H(z')$ becomes

$$H(z') = \frac{-0.5243z' - 0.5243}{1.00974z' - 0.99026} \quad (\text{eqn 2.58})$$

Equation 2.58 is shown in Figure 2.11 and Figure 2.12

Finally Figure 2.13 shows the output of the practical circuit of Figure 2.6. The experimental result perfectly matches all the computer simulations outputs of Figure 2.7 through Figure 2.12. Furthermore, a smoothing low-pass filter is connected to the output of the practical circuit to get rid of the clock feedthrough problem mentioned in Chapter I.

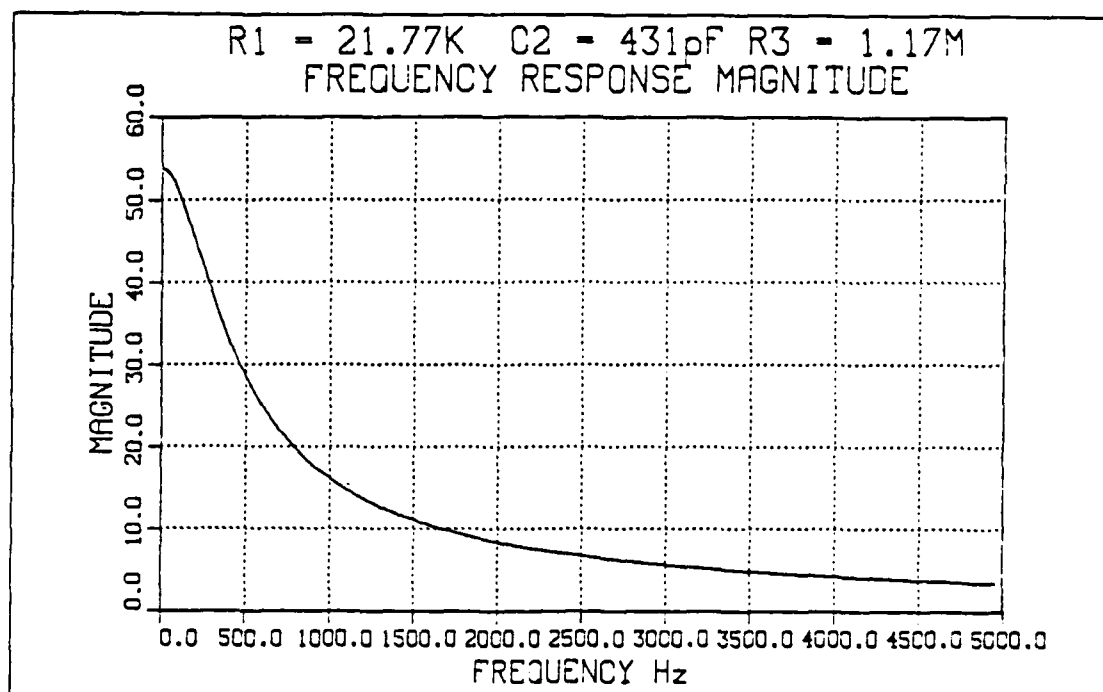


Figure 2.7 Computer Simulation of Lossy Integrator in s-Domain (Magnitude).

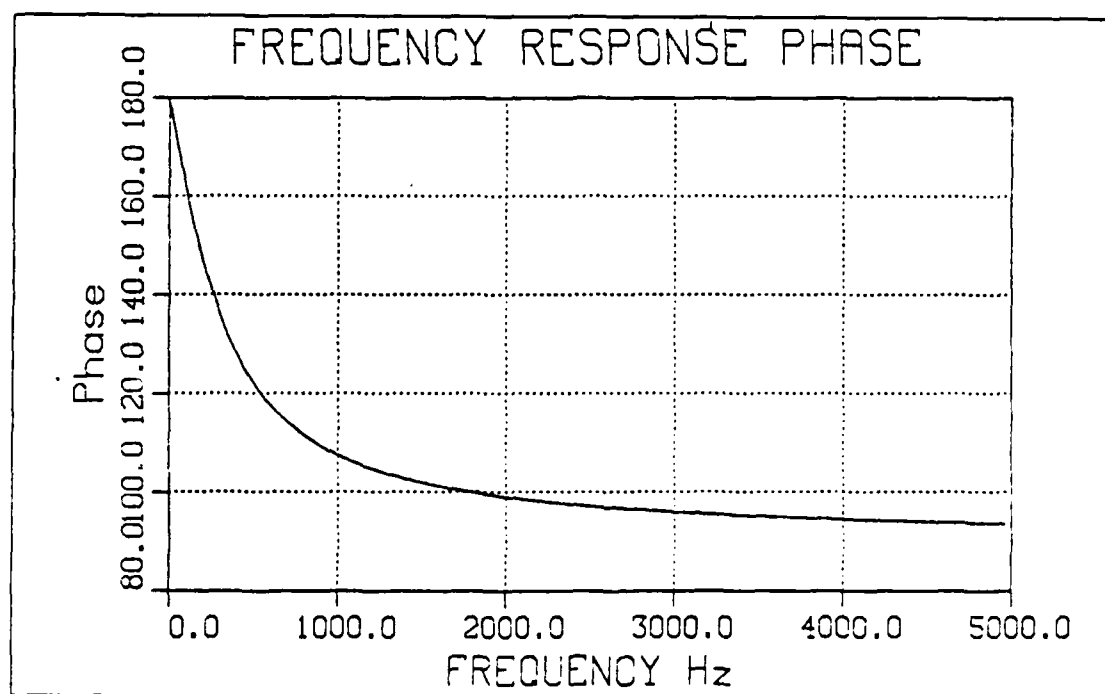


Figure 2.8 Computer Simulation of Lossy Integrator in s-Domain (Phase).

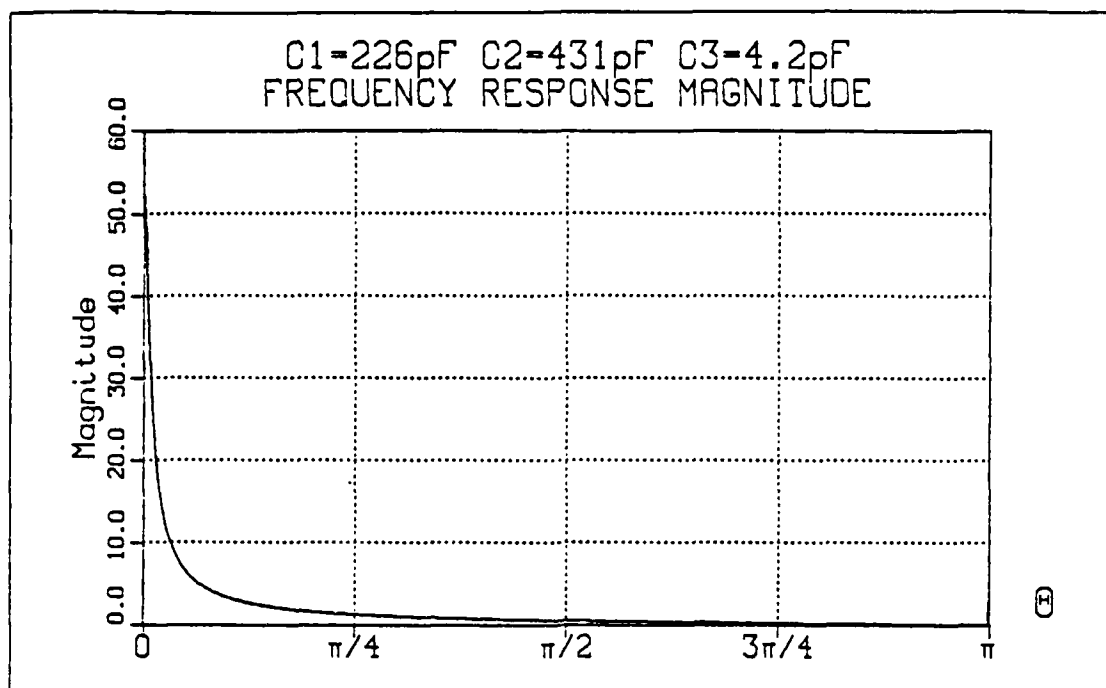


Figure 2.9 Computer Simulation of Lossy Bilinear Integrator in z-Domain (Magnitude).

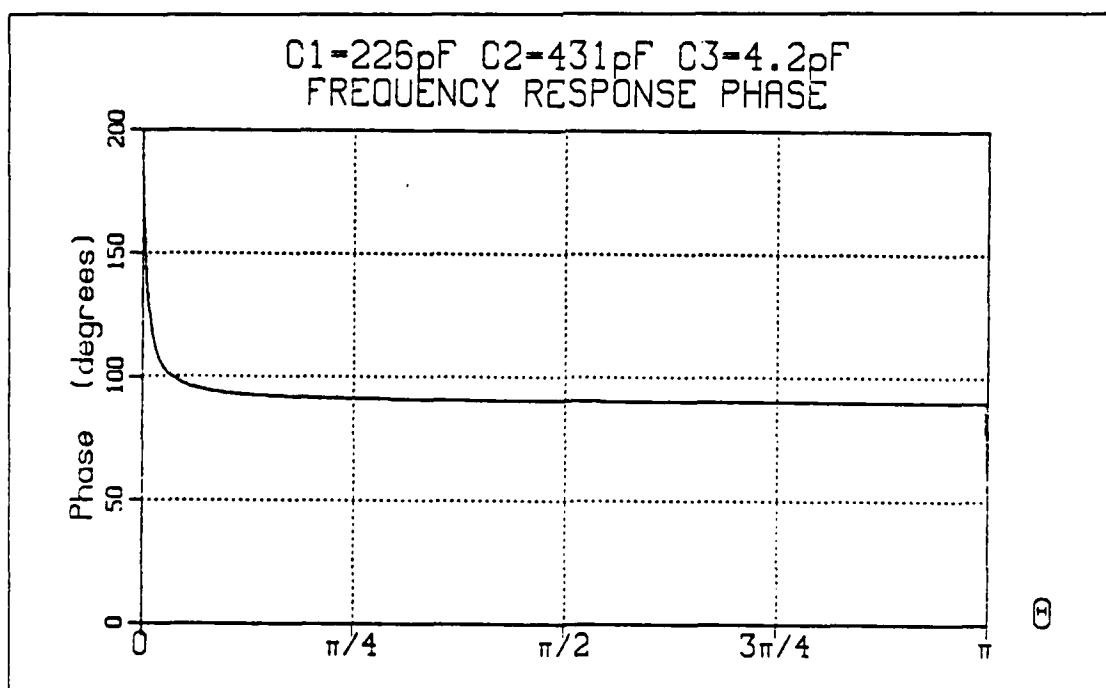


Figure 2.10 Computer Simulation of Lossy Bilinear Integrator in z-Domain (Phase).

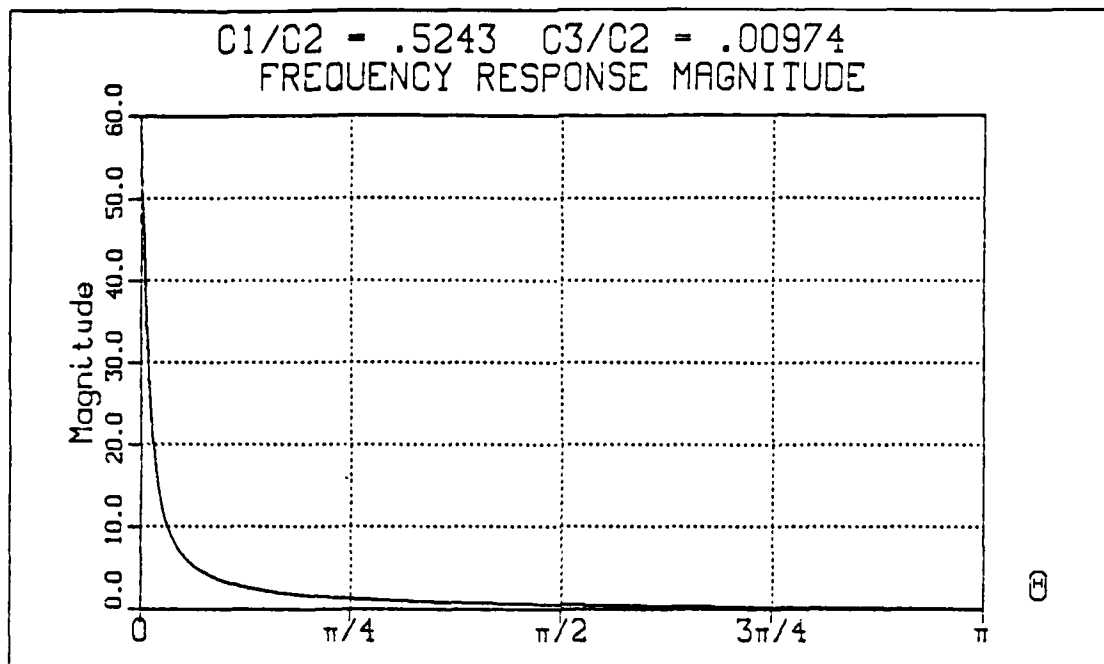


Figure 2.11 Computer Simulation of Lossy Bilinear Integrator
Using Building Blocks Approach (Magnitude).

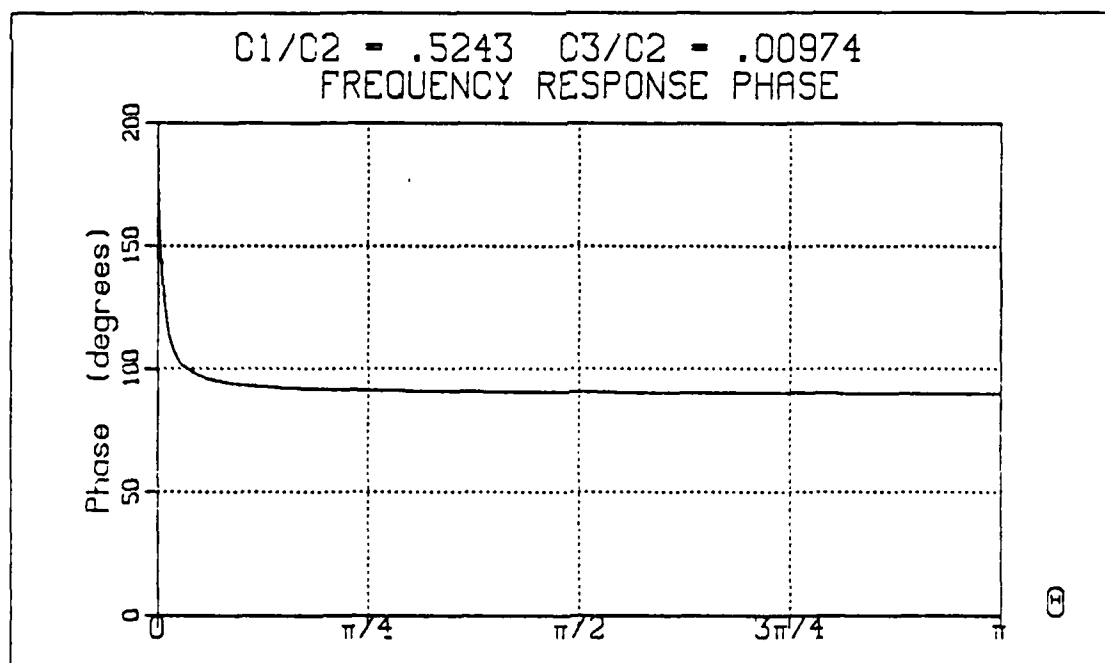


Figure 2.12 Computer Simulation of Lossy Bilinear Integrator
Using Building Blocks Approach (Phase).

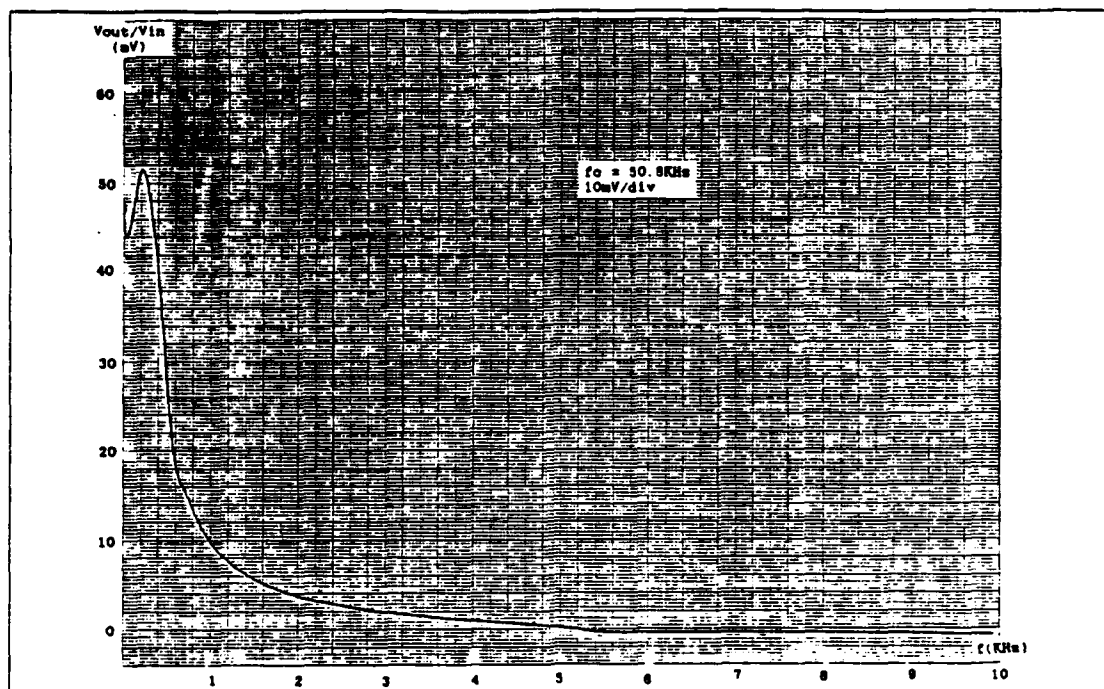


Figure 2.13 Experimental Result of Lossy Bilinear Integrator.

These results showed that the following design steps can be used to meet the given specifications.

1. Definitions of the filter specifications in the frequency domain.
2. Construction of the continuous transfer function $H(s)$.
3. Transformation from $H(s)$ to $H(z')$ using bilinear mapping technique.
4. Use of building block approach as implementation.
5. Finally construction of switched capacitor realization of the filter. Or after step 2.
6. Resistor simulation of the continuous resistance.
7. Go to step 5 (taking into account nonideal properties of the SC networks).

The most important outcome of this experiments is the different approaches one can use to simulate continuous resistance using bilinear switched capacitor realization. In one approach the bilinear transformation is used through the step 1, 2, 3, 4, 5. The other approach would yield the same results using steps 1, 2, 6, 3, 7. This fact is shown in Figure 2.11 and Figure 2.9 respectively.

III. PROGRAMMABLE GIC SC FILTER

A. GENERAL

The programmable filter is a very interesting and useful application of the SC networks. This is due to the fact that the SC circuit's frequency response can be changed by varying clock frequency. In fact a remarkable feature is that, multiplying the clock frequency by a factor α results in scaling the frequency response (multiplied) by the *same factor* along the frequency axis.

Most of the active SC networks have limitation over the clock frequency range, depending on the operational amplifier's settling time used in the circuit. In today's technology, MOS op. amps. can be designed with 0.5 μ sec settling time to reach 0.1% of its final value of the step response. Clock rates up to 1 MHz seem feasible. In practice, MOS op. amps. has been designed which settle to within 0.1% of the final value in 2 μ sec and achieve dc gains greater than 60 dB. Therefore sampling rates of up to 250 KHz, can be easily achieved. Considering the Nyquist criteria, almost a 100 KHz signal can be processed using SC networks, if the op-amp slew rate is not taken into account.

The design approach used in this research, in general, is the extension of the design explained in [Ref. 6]. It addresses three different aspects of programmability. These are

1. Programming the filter topology using a minimal set of elements to obtain any type of filtering function desired, for example LP, HP, BP, N and AP, by using a binary control word.
2. Programming the filter's transfer function parameters (pole resonant frequency and quality factor) for a chosen type of filtering function by using a digital control word.
3. Reprogramming the filter's transfer function parameters by changing the clock frequency (practically from 50 KHz to 250 KHz).

B. THE PROPOSED GIC SC PROGRAMMABLE FILTER

The basic active network considered as the heart of the GIC SC programmable filter is the Generalized Immittance Converter (GIC) structure [Ref. 7] of Figure 3.1, whose superior performance was established in the [Ref. 8] and [Ref. 9]. The filters transfer functions derived can be found in [Ref. 6].

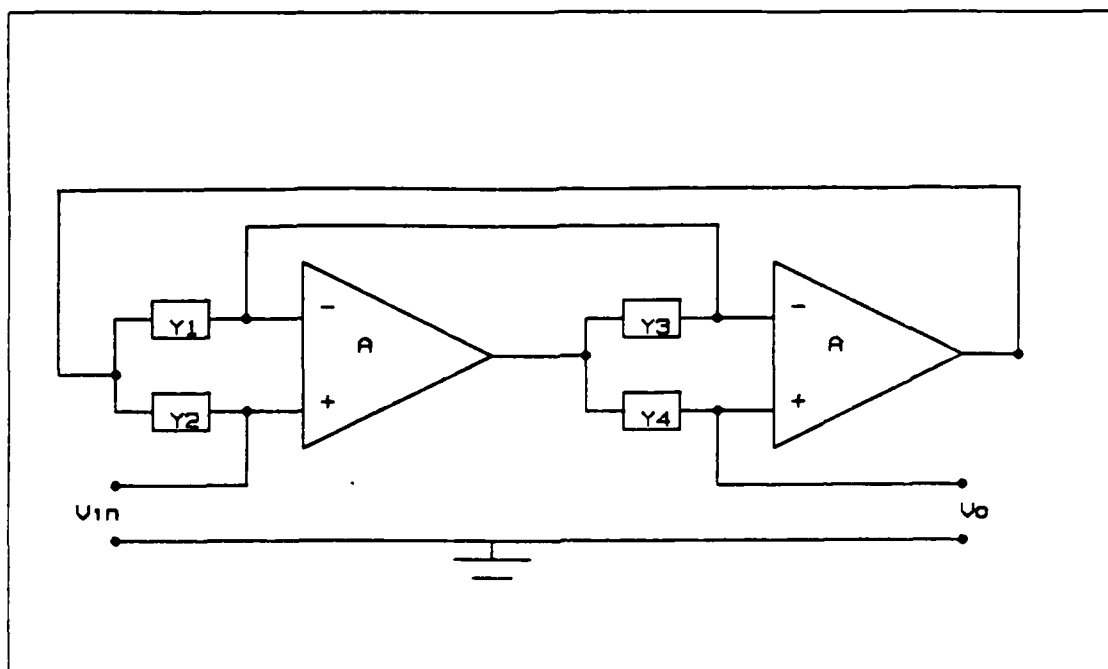


Figure 3.1 The GIC Implementation Using Op. Amps..

The bilinear realization of a continuous resistance was used throughout the design. Table 1, illustrates that for any filter realization, five switched capacitors, two unswitched capacitors, and two op. amps. are required. G stands for the admittance represented by switched capacitor.

The passive elements are connected to the different nodes, shown in Figure 3.2, for the different realizations. A set of MOS bilateral switches controlled by a digital binary word are used to interchange the elements to achieve the different types of filter realization. The truth table of the switch control logics is shown in Table 2. Figure 3.3 illustrates the CMOS logic circuit used for realizing this truth table.

Four of the five switched capacitors are equal and of value C_{eq} each, the fifth switched capacitor is the Q_p determining capacitor and of value $C_q = C_{eq} Q_p$. Other two capacitors in the circuit are equal, and of value $C = 4f_c C_{eq} w_p$ each. The two equal banks of capacitors are used to control w_p . Each bank contains n binary weighted capacitors connected in parallel through analog CMOS switches as shown in Figure 3.4. Using a digital binary word of n bits to control w_p , 2^n different values of C will result at the 2 terminals of both capacitor banks that correspond to 2^n different values of w_p .

TABLE 1
THE ELEMENTS IDENTIFICATION FOR DIFFERENT
REALIZATIONS OF THE GIC FILTER

Filter Type	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8
LP	G	C	$C + \frac{G}{Q_P}$	G	G	0	0	G
HP	G	G	C	G	0	G	C	$\frac{G}{Q_P}$
BP	G	G	C	G	0	G	$\frac{G}{Q_P}$	C
N	G	G	C	G	G	0	C	$\frac{G}{Q_P}$
AL	G	G	C	G	G	0	C	$\frac{G}{Q_P}$

Using a similar technique the value of C_q can be controlled through a bank of m binary weighted capacitors in parallel through analog CMOS switches as shown in Figure 3.5. Using a digital binary word of m bits to control Q_p , 2^m different values of C_q can be achieved that correspond to 2^m different values of Q_p . Thus, full independent control of the pole pair w_p and Q_p are achieved by programming the switches to obtain the corresponding C and C_q .

C. THE REALIZED GIC SC PROGRAMMABLE FILTER

The detailed diagram of the signal processing circuit of the constructed GIC SC filter is shown in Figure 3.6. The value of m and n were selected $m=n=4$. Thus, 15 different values of w_p (f_p) and Q_p were obtained as it is illustrated at the corresponding Table 3 and Table 4. The implemented banks for the control of w_p and Q_p are shown in Figure 3.7 and Figure 3.8 with their values. The clock frequency is 101 KHz throughout the design. According to this clock frequency, the switched capacitors value were chosen within range from 500 pF to 8nF, using experimental result of Chapter I Figure 1.15.

TABLE 2
THE TRUTH TABLE OF THE SWITCHES LOGIC USED
TO SELECT THE FILTERING FUNCTION

Binary Input	Switch		S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	S ₉	S ₁₀	S ₁₁	S ₁₂	S ₁₃	S ₁₄	S ₁₅	S ₁₆	S ₂₉	S ₃₀	
	Filter																				
0 0 0	Low Pass		0	1	0	1	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0
0 0 1	High Pass		1	0	1	0	0	1	0	0	0	1	0	1	0	1	0	1	1	0	0
0 1 0	Band Pass		1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	1	0	0
0 1 1	Notch		0	1	1	0	0	1	0	0	0	1	0	1	0	1	1	0	0	1	0
1 0 0	All Pass		0	1	1	0	0	1	0	0	0	1	0	1	0	1	1	0	1	0	0

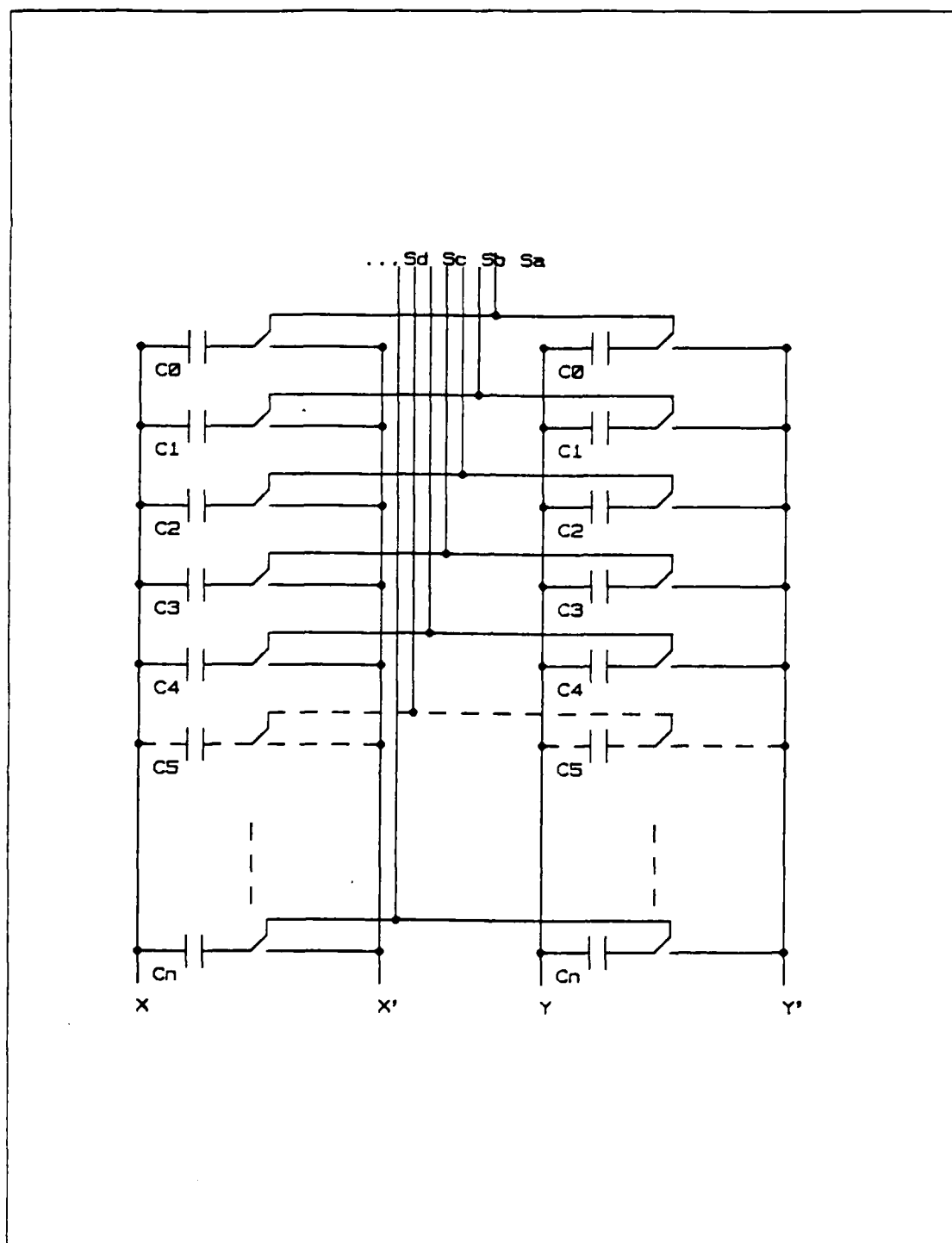


Figure 3.4 The Two Capacitor Banks Realization for the Programming of w_p .

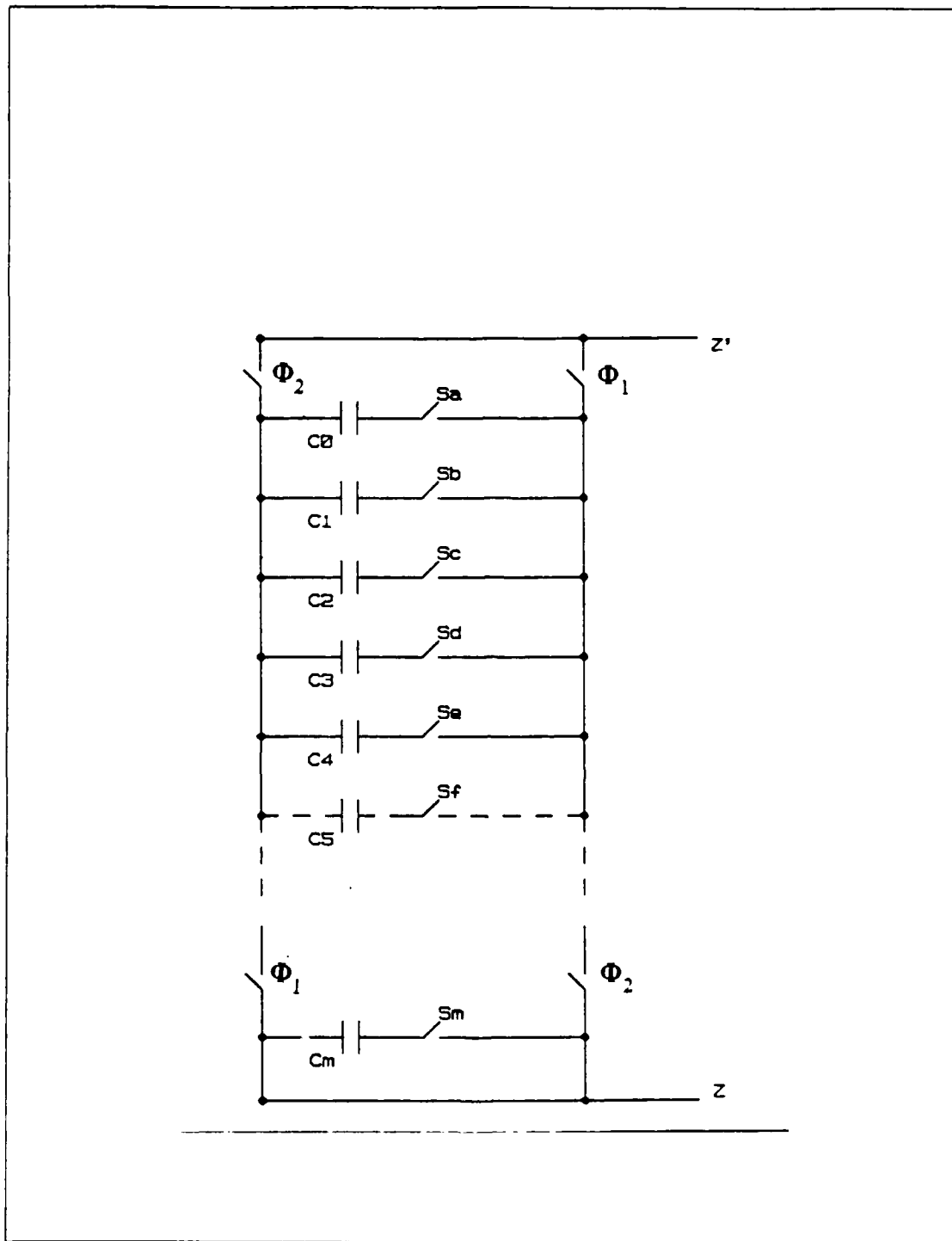


Figure 3.5 The Capacitor Bank for the Programming of Q_p .

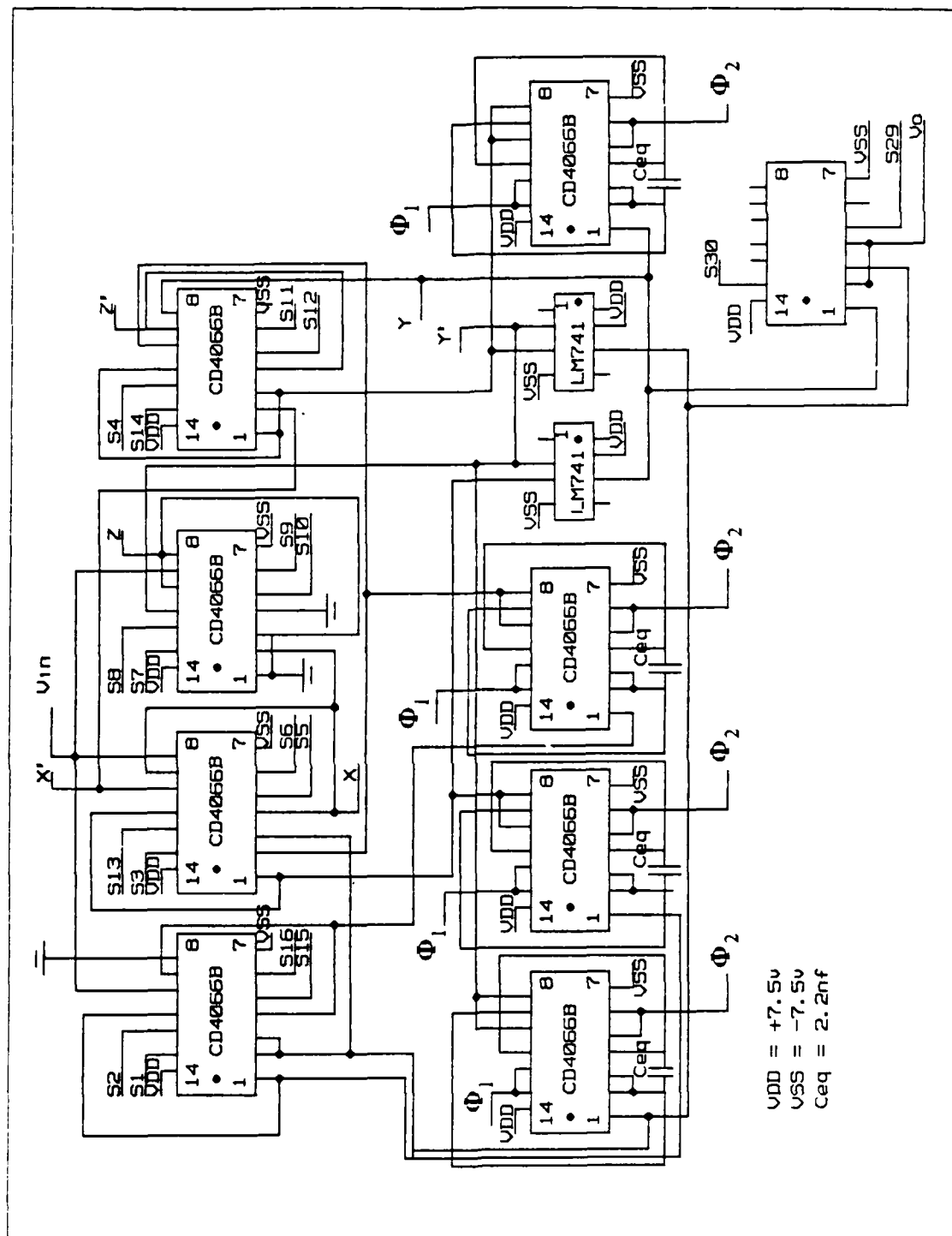


Figure 3.6 The Detailed Design of Signal Processing Circuit.

TABLE 3
THE FOUR-BIT WORDS THAT CONTROL $W_p (F_p)$

Sd	Sc	Sb	Sa	IDEAL nf	ON CIRCUIT nf	POLE FREQUENCY KHz
0	0	0	0	—	—	—
0	0	0	1	5	4.9	30.35
0	0	1	0	10	10.4	14.3
0	0	1	1	15	15.3	9.72
0	1	0	0	20	19.7	7.55
0	1	0	1	25	24.7	6.02
0	1	1	0	30	30.1	4.94
0	1	1	1	35	35	4.25
1	0	0	0	47	46.9	3.17
1	0	0	1	52	51.8	2.87
1	0	1	0	57	57.3	2.595
1	0	1	1	62	62.2	2.391
1	1	0	0	67	66.6	2.23
1	1	0	1	72	71.5	2.08
1	1	1	0	77	77	1.93
1	1	1	1	82	81.9	1.81
CLOCK FREQUENCY = 101KHz						

TABLE 4
THE FOUR-BIT WORDS THAT CONTROL Q_p

Sd	Sc	Sb	Sa	IDEAL pf	ON CIRCUIT pf	QUALITY FACTOR Q
0	0	0	0	—	—	—
0	0	0	1	150	148	15.54
0	0	1	0	300	295	7.796
0	0	1	1	450	443	5.192
0	1	0	0	550	508	4.52
0	1	0	1	710	656	4.070
0	1	1	0	860	803	2.864
0	1	1	1	1010	951	2.41
1	0	0	0	1000	1090	2.11
1	0	0	1	1150	1238	1.8578
1	0	1	0	1300	1385	1.66
1	0	1	1	1450	1533	1.5
1	1	0	0	1550	1533	1.5
1	1	0	1	1710	1681	1.368
1	1	1	0	1850	1828	1.258
1	1	1	1			
CLOCK FREQUENCY = 101KHz						

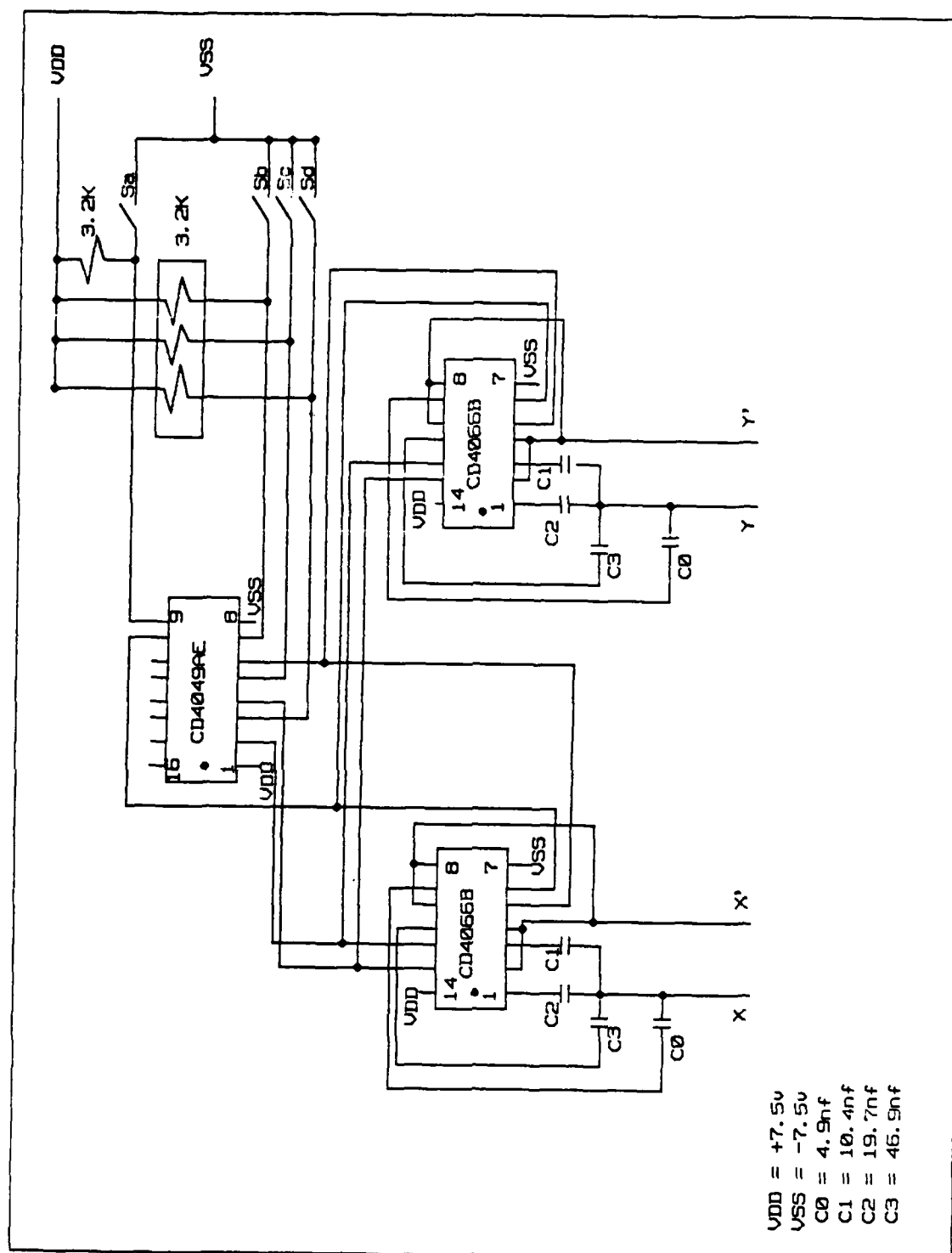


Figure 3.7 The Implemented Capacitor Bank for $w_p(f_p)$.

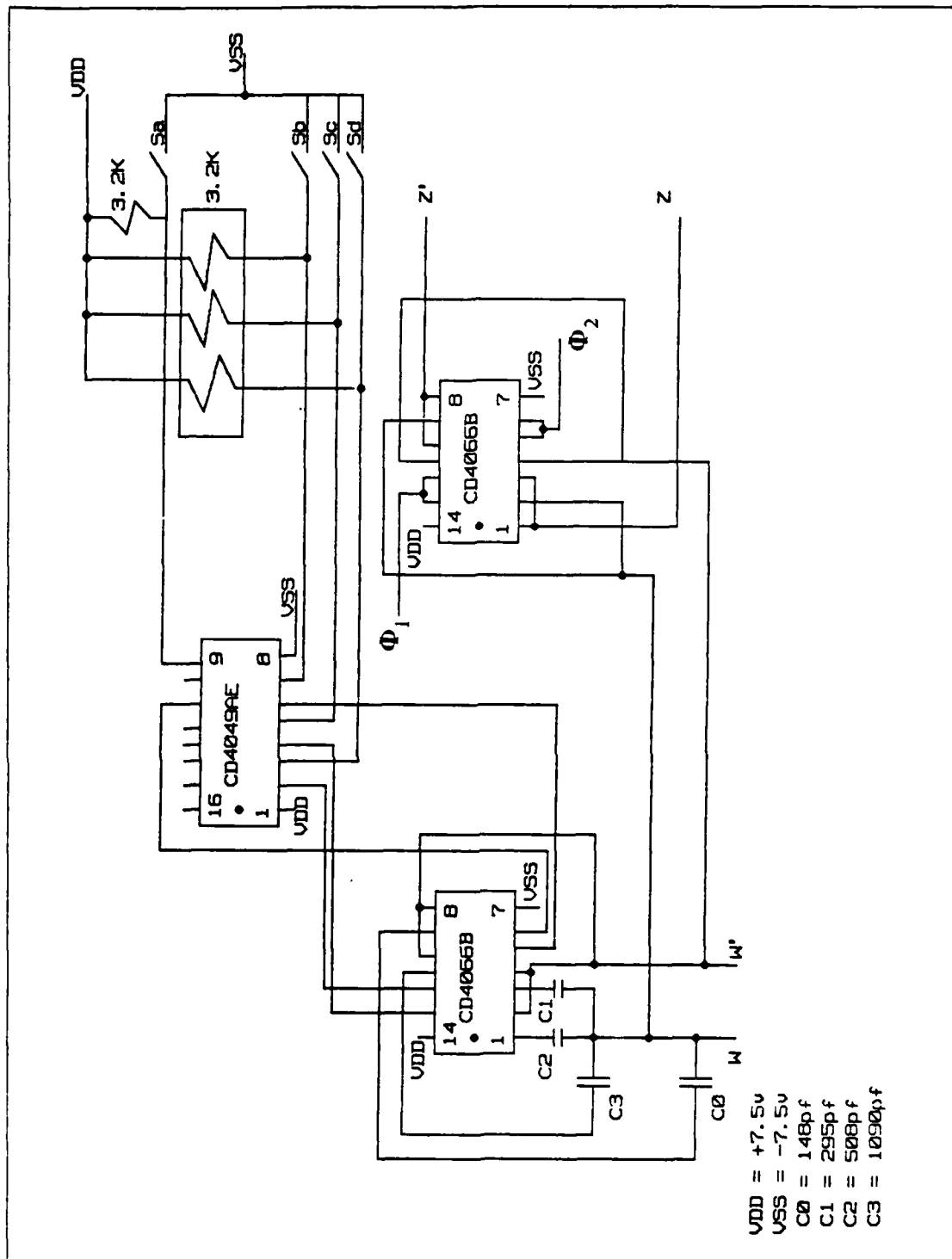


Figure 3.8 The Implemented Capacitor Bank for Q_p .

IV. COMPUTER SIMULATION OF THE PROPOSED GIC ACTIVE FILTER

A. INTRODUCTION

In order to observe the theoretical frequency responses of the different realizations, that is LP, HP, BP, N and AP, with different pole frequencies and quality factors, the computer program, GICFRQ, has been written in FORTRAN programming language. The Display Integrated Software System and Plotting Language (DISSPLA) has been used to produce the desired graphic output. This frequency response program is shown in Appendix B. As it is seen this program, accepts some inputs from a data file, related with the transfer function of the realization. These inputs are processed through the program and results are passed to DISSPLA to draw the graph. One can plot the phase responses of the realizations as well as the magnitude responses by making minor changes in the DISSPLA package.

Because of the two four-bit control words for each realization, there will be a rather large number of input sets. For this reason a few intermediate control words were picked up randomly. In order to compare the computer simulations to the experimental results, the same control words are going to be chosen in next chapter.

B. SIMULATION RESPONSE(S)

1. Low Pass Filter Realization

Using the elements values prescribed in Table 1 yields the following low pass filter transfer function

$$H(s) = \frac{2W_p^2}{s^2 + (W_p/Q_p)s + W_p^2} \quad (\text{eqn 4.1})$$

First, it is assumed that the control word for Q_p is set to 1010 which corresponds to $Q_p = 1.66$ as shown in Table 4. Then Figure 4.1 through Figure 4.3 are plotted by varying the $W_p(f_p)$ to illustrate the magnitude responses of the ideal LPF GIC realization. Second, the control word W_p is set to 1010 which corresponds to $f_p = 2.595$ KHz as shown in Table 3. Then Figure 4.4 are plotted for $Q_p = 2.11$, $Q_p = 4.07$, $Q_p = 5.192$.

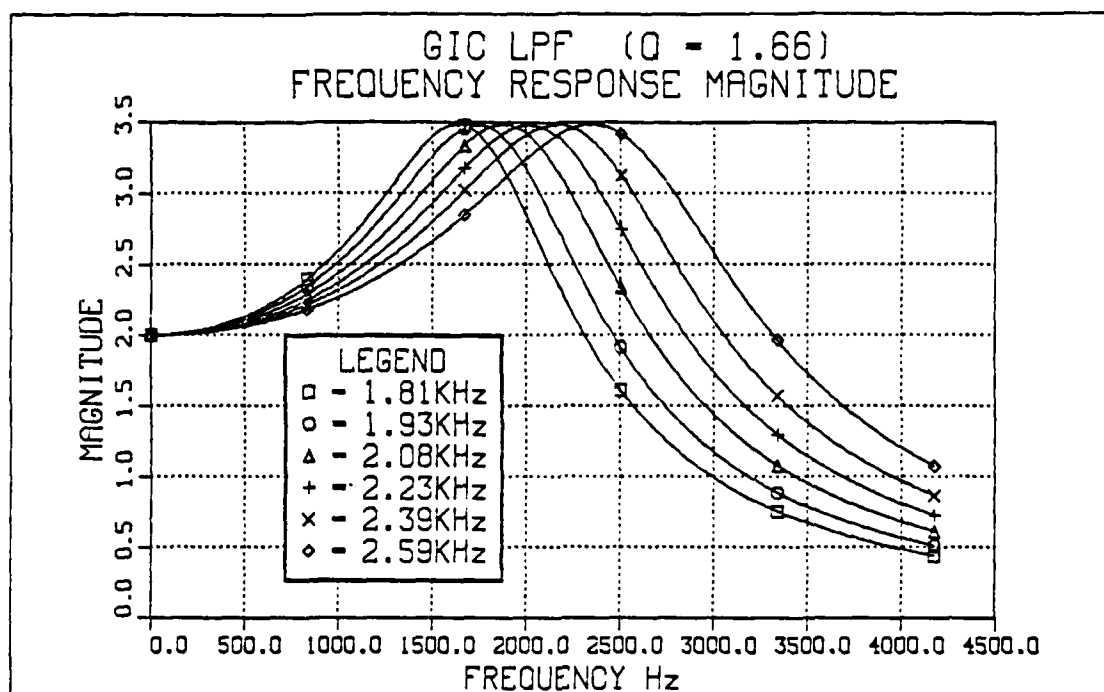


Figure 4.1 Ideal GIC LPF Magnitude Response.

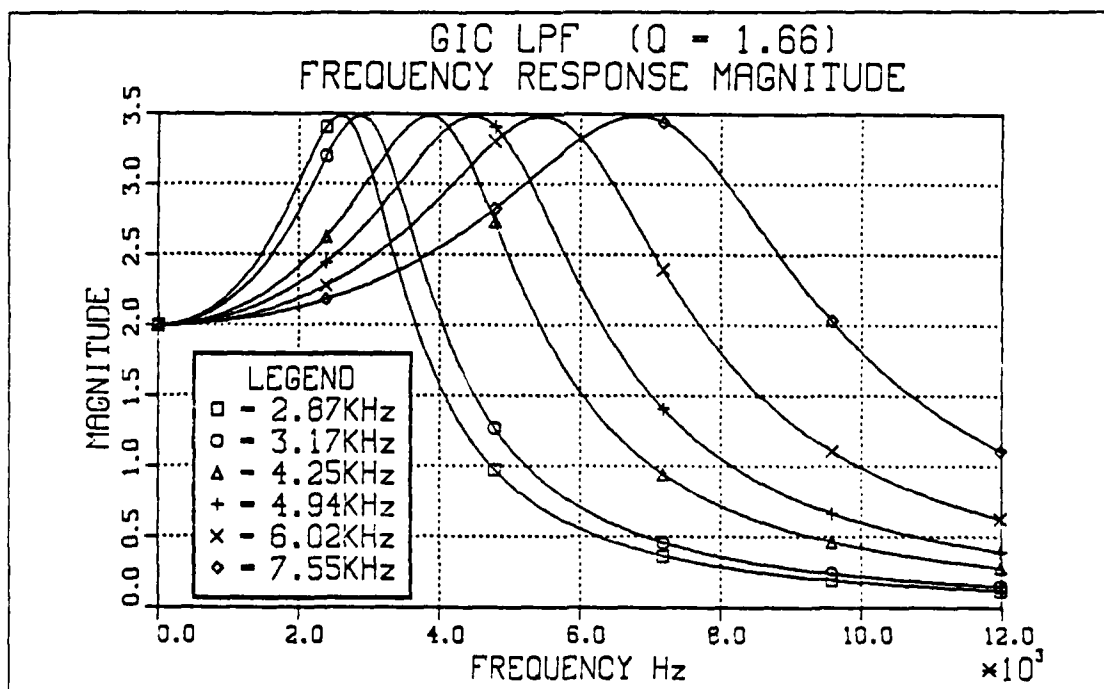


Figure 4.2 Ideal GIC LPF Magnitude Response.

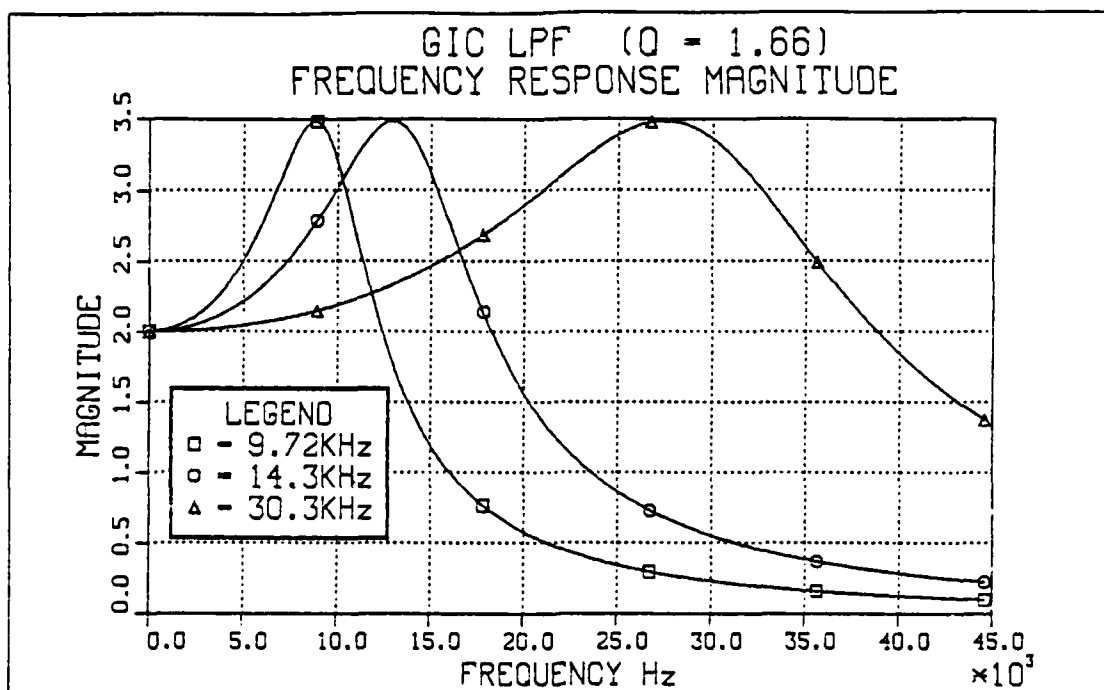


Figure 4.3 Ideal GIC LPF Magnitude Response.

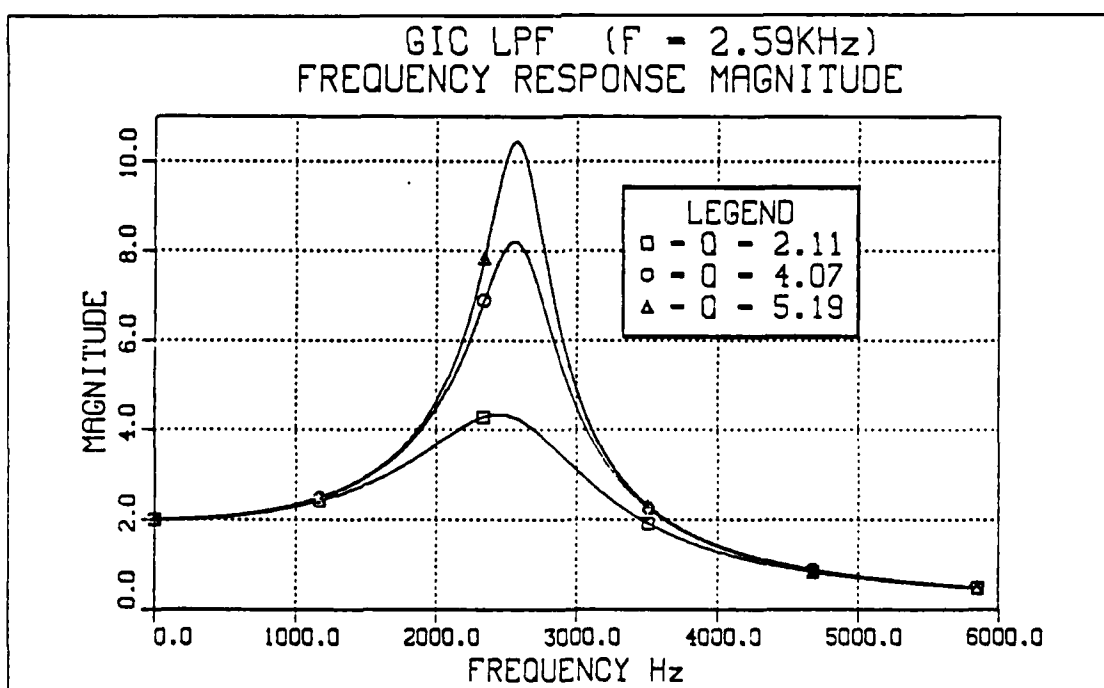


Figure 4.4 Ideal GIC LPF Magnitude Response with Different Q_p s.

2. High Pass Filter Realization

Using the elements value shown in Table 1 yields the following high pass filter transfer function

$$H(s) = \frac{2s^2}{s^2 + (W_p \cdot Q_p)s + W_p^2} \quad (\text{eqn 4.2})$$

If we do the same set up as we did for the low pass filter case, we can obtain the various magnitude response curves shown in Figure 4.5 through Figure 4.7. Figure 4.8 illustrates the effect of changing Q_p on filter response. The same quality factor was especially chosen as in the case of the low pass filter, because similarities and differences can be illustrated more apperant in this fashion.

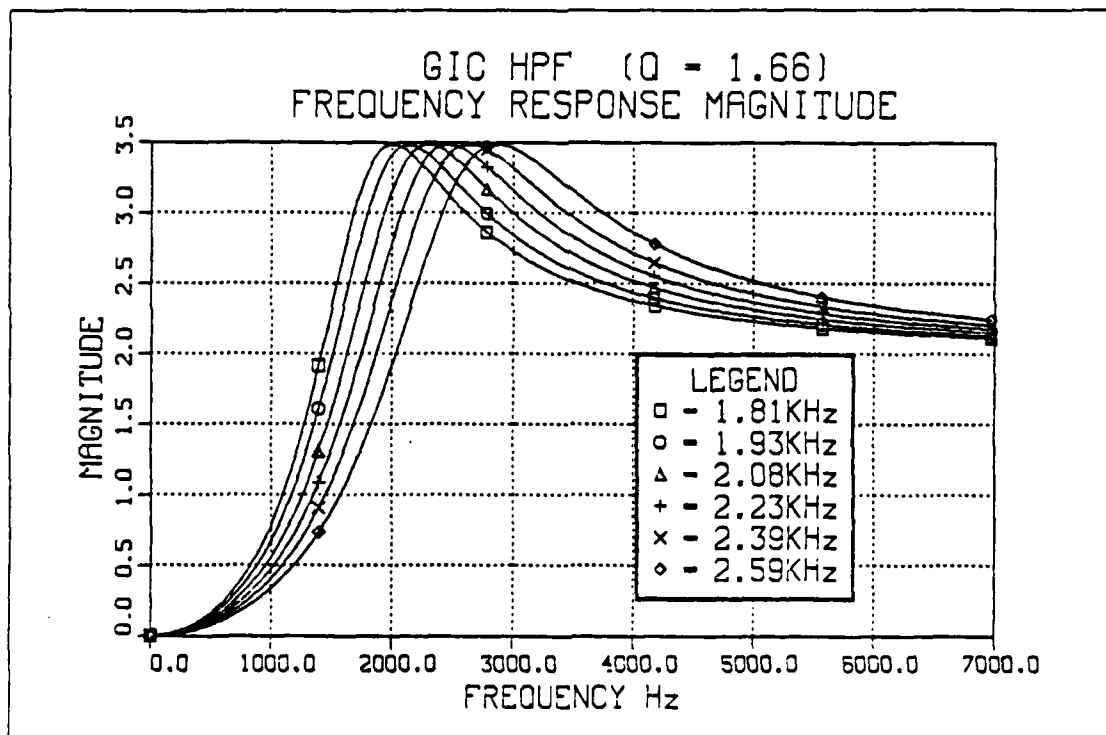


Figure 4.5 Ideal GIC HPF Magnitude Response.

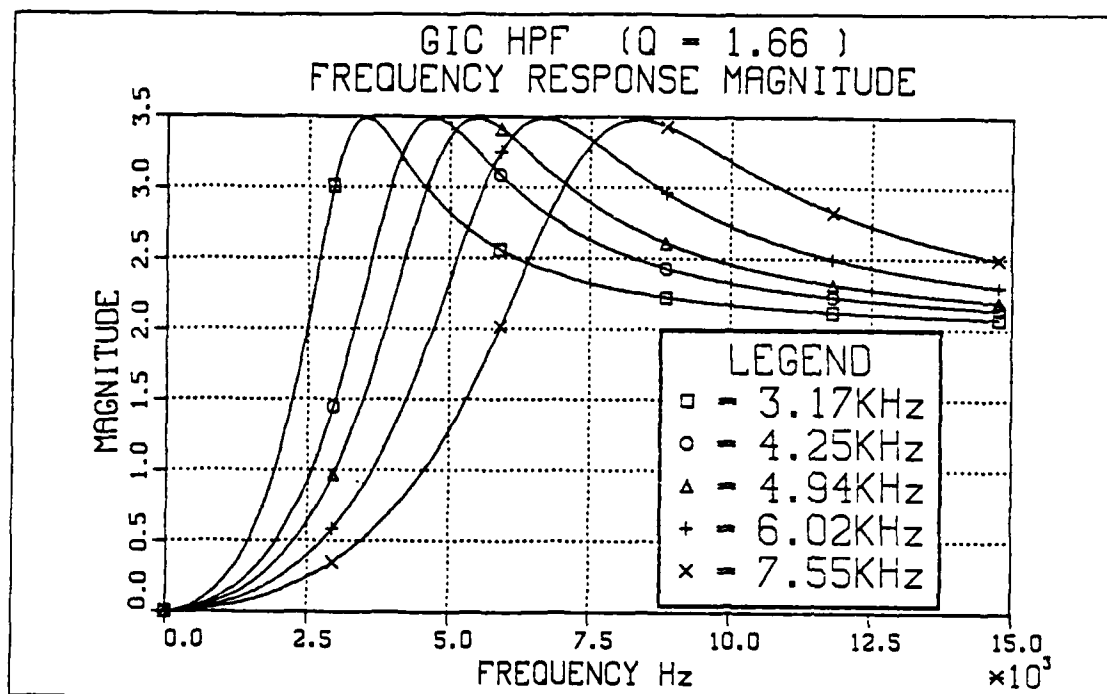


Figure 4.6 Ideal GIC HPF Magnitude Response.

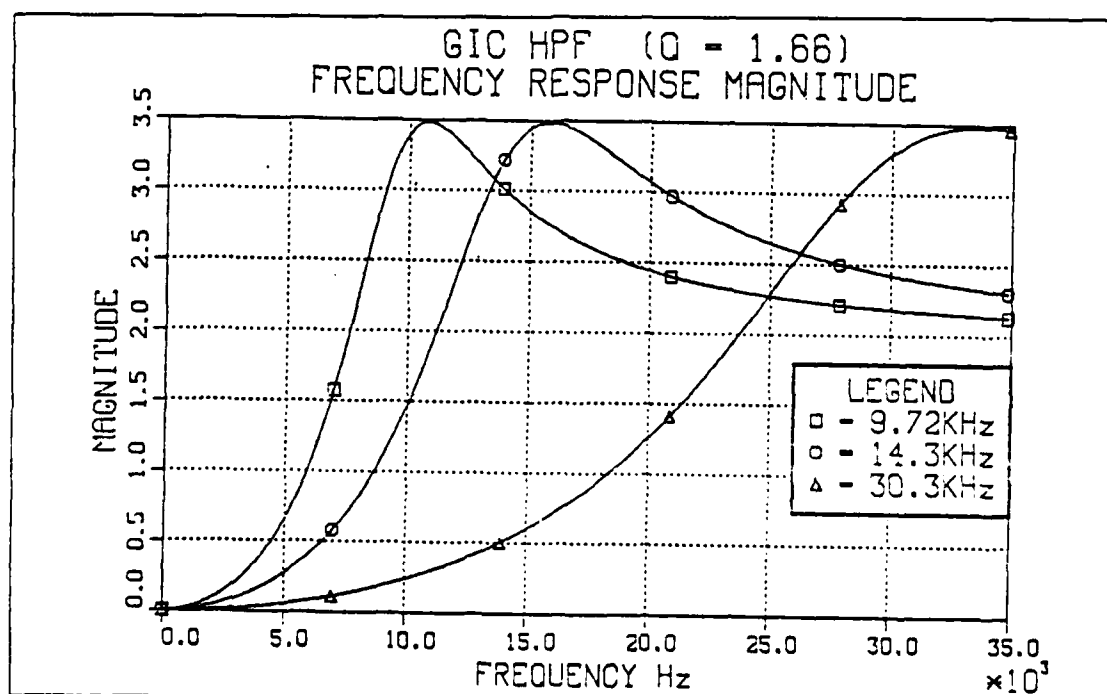


Figure 4.7 Ideal GIC HPF Magnitude Response.

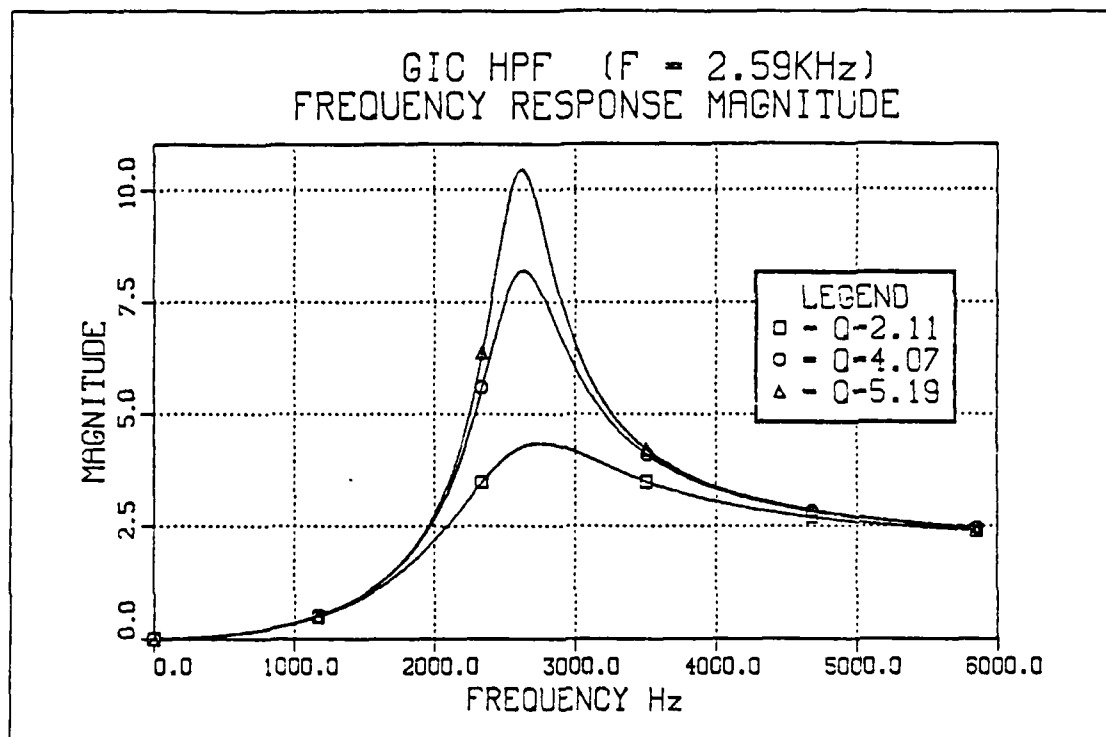


Figure 4.8 Ideal GIC HPF Magnitude Response with Different Q_p s.

3. Band Pass Filter Realization

The band pass transfer function of the GIC filter is

$$H(s) = \frac{2(W_p/Q_p)s}{s^2 + (W_p/Q_p)s + W_p^2} \quad (\text{eqn 4.3})$$

This will correspond to a gain of two at the pole frequency

$$H(jW_p) = 2$$

BPF realization is simulated for various $W_p(f_p)$ when $Q_p = 4.52$ in Figure 4.9 and Figure 4.10. Figure 4.11 shows the magnitude response of BPF with different quality factors namely $Q_p = 5.192$, $Q_p = 7.796$ and $Q_p = 15.54$ with W_p held constant. All figures show that the maximum gain at the pole frequency (W_p) is 2 independent of the quality factor.

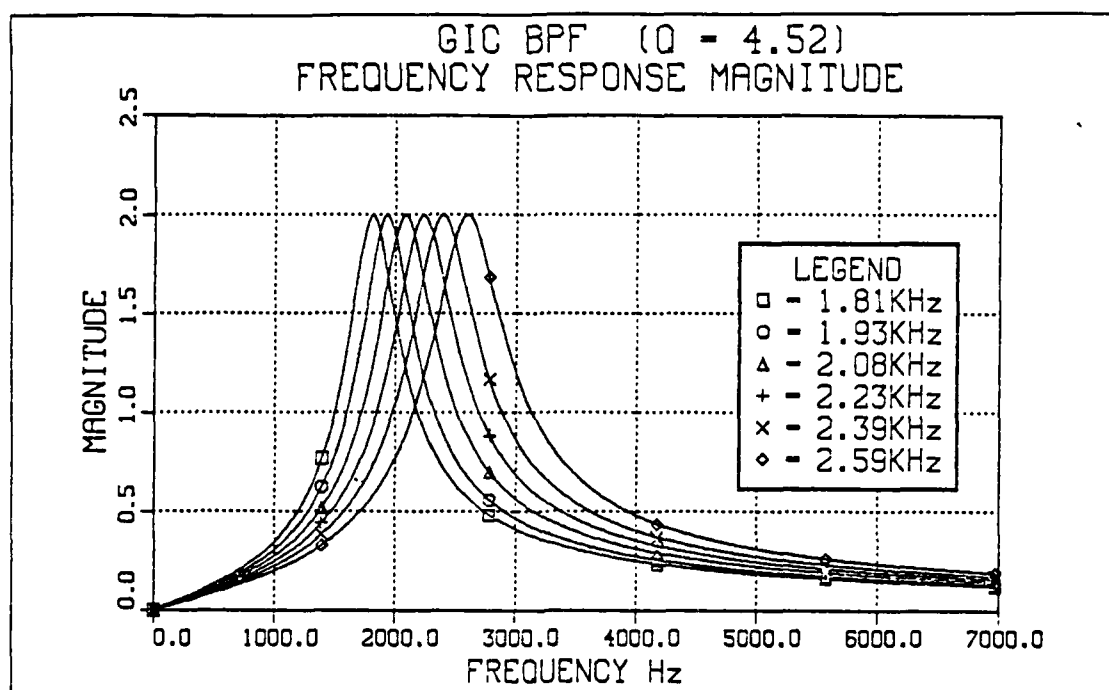


Figure 4.9 Ideal GIC BPF Magnitude Response.

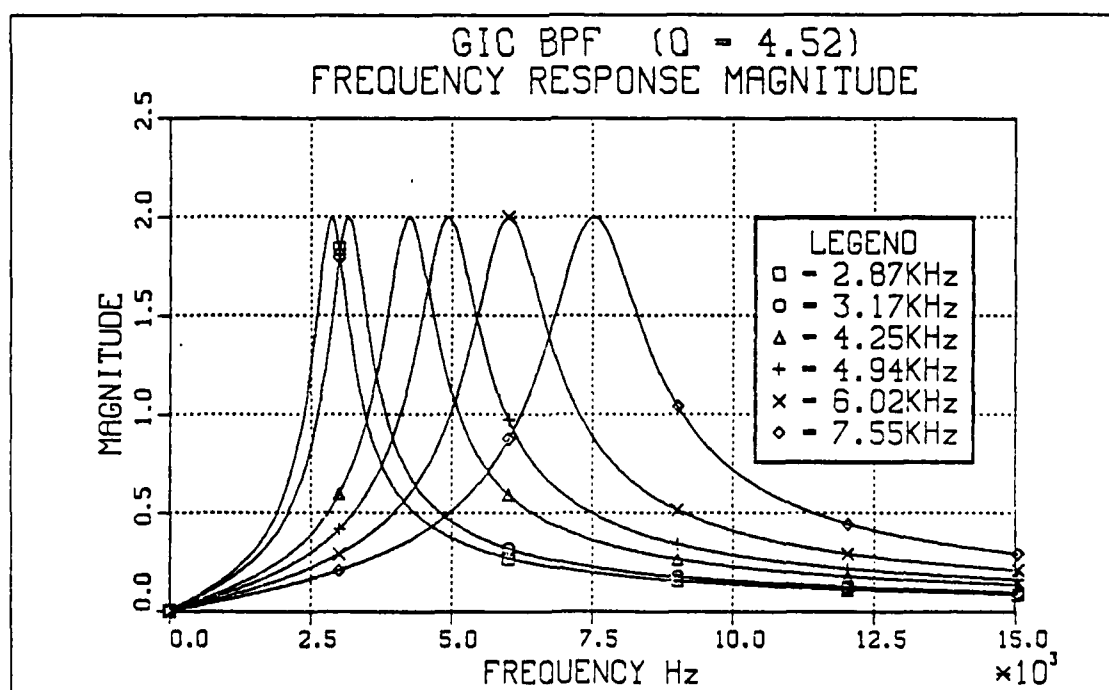


Figure 4.10 Ideal GIC BPF Magnitude Response.

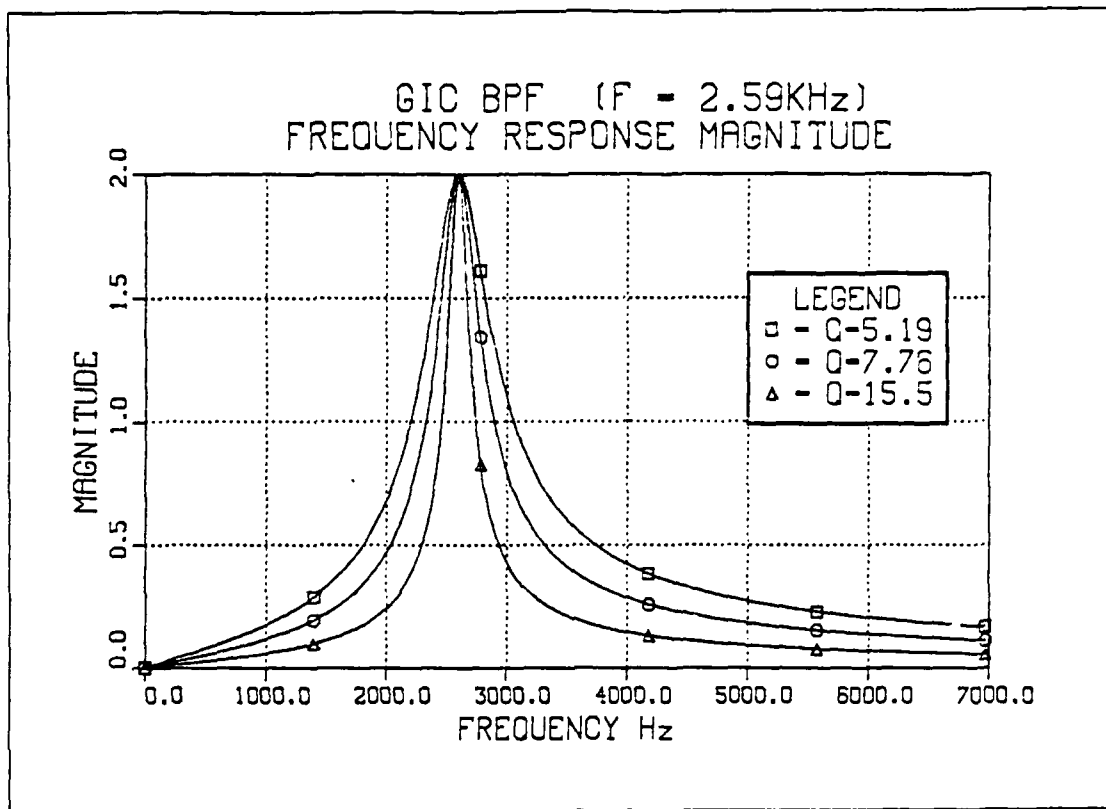


Figure 4.11 Ideal GIC BPF Magnitude Response with Different Q_p s.

4. Notch Filter Realization

Using appropriate element combination, a notch filter transfer function can be obtained as

$$H(s) = \frac{s^2 + W_n^2}{s^2 + (W_p Q_p) + W_p^2} \quad (\text{eqn 4.4})$$

Figure 4.12 illustrates the ideal notch filter amplitude response for a variety of frequencies with constant Q_p , $Q_p = 1.66$, while Figure 4.13 for a variety of Q_p s with constant $W_p(f_p)$. The notch frequency, W_n , is determined by both pole frequency and quality factor. As it is shown in the figures, if one of the parameters is held as constant the notch frequency still will continue to shift along the frequency axis.

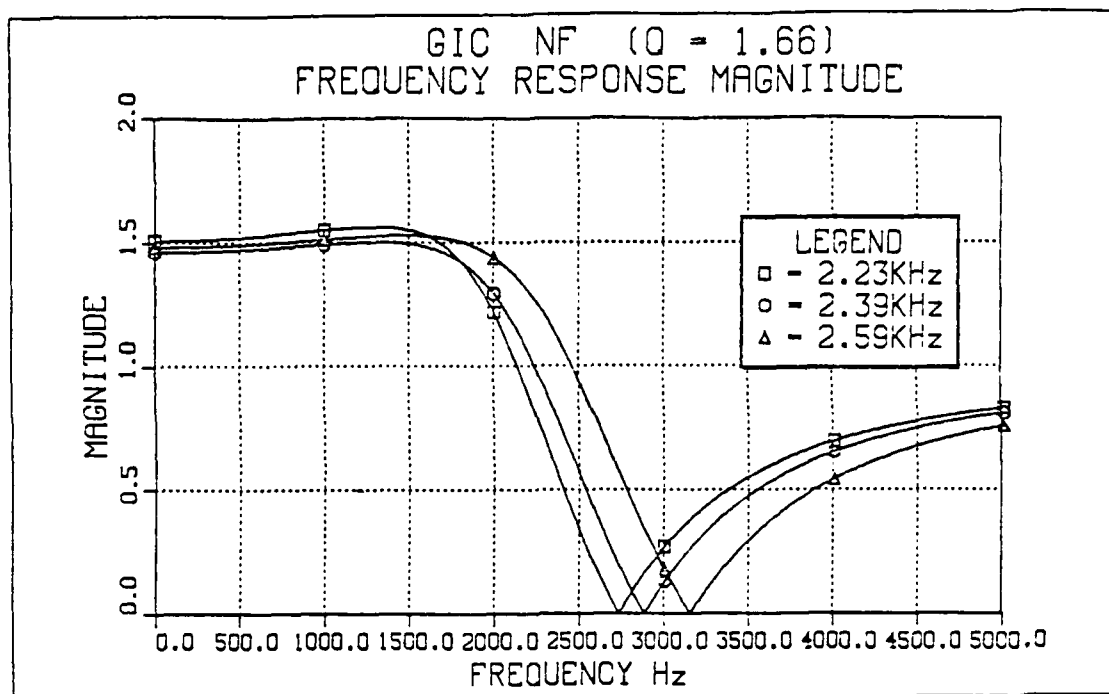


Figure 4.12 Ideal GIC NF Magnitude Response.

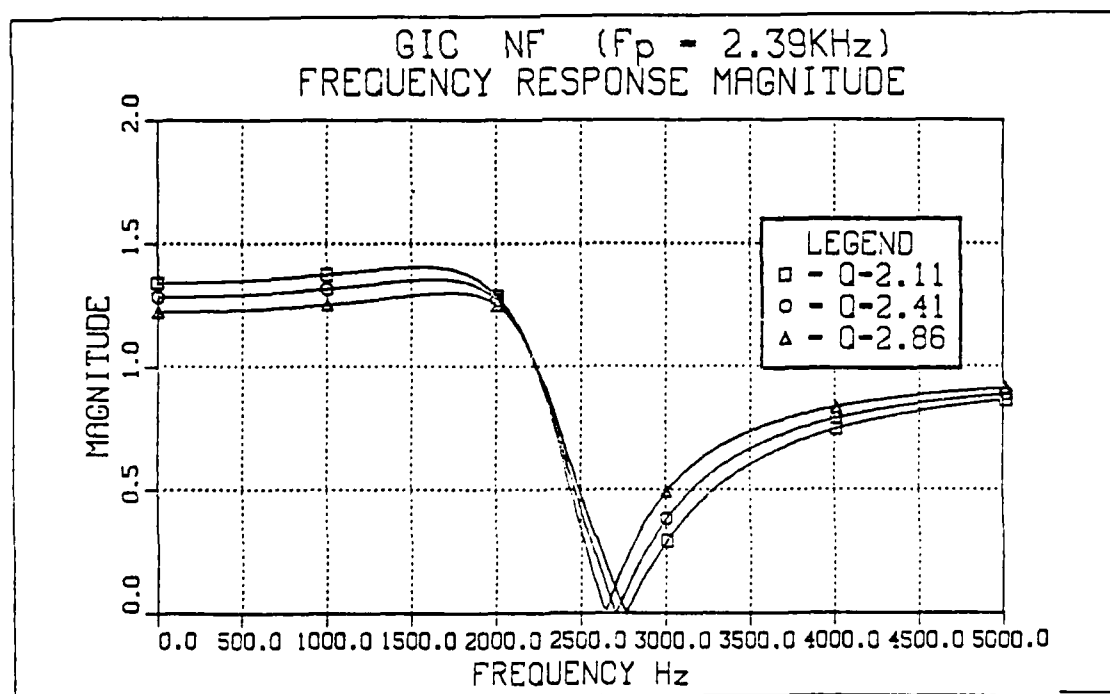


Figure 4.13 Ideal GIC NF Magnitude Response with Different Q_p s.

5. All Pass Filter Realization

As proposed in Table 1 using the same element values as in the notch filter case but different output node, all pass filter transfer function can be derived as

$$H(s) = \frac{s^2 - (W_p \cdot Q_p)s + W_p^2}{s^2 + (W_p \cdot Q_p)s + W_p^2} \quad (\text{eqn 4.5})$$

which takes the value of Magnitude $\rightarrow 1$ as ideal amplitude response. All pass transfer functions are often needed for delay equalization, that is, the phase response of the circuit has to have 360° shifting property around the pole frequency, f_p . This property agree with the computer simulation result shown in Figure 4.14.

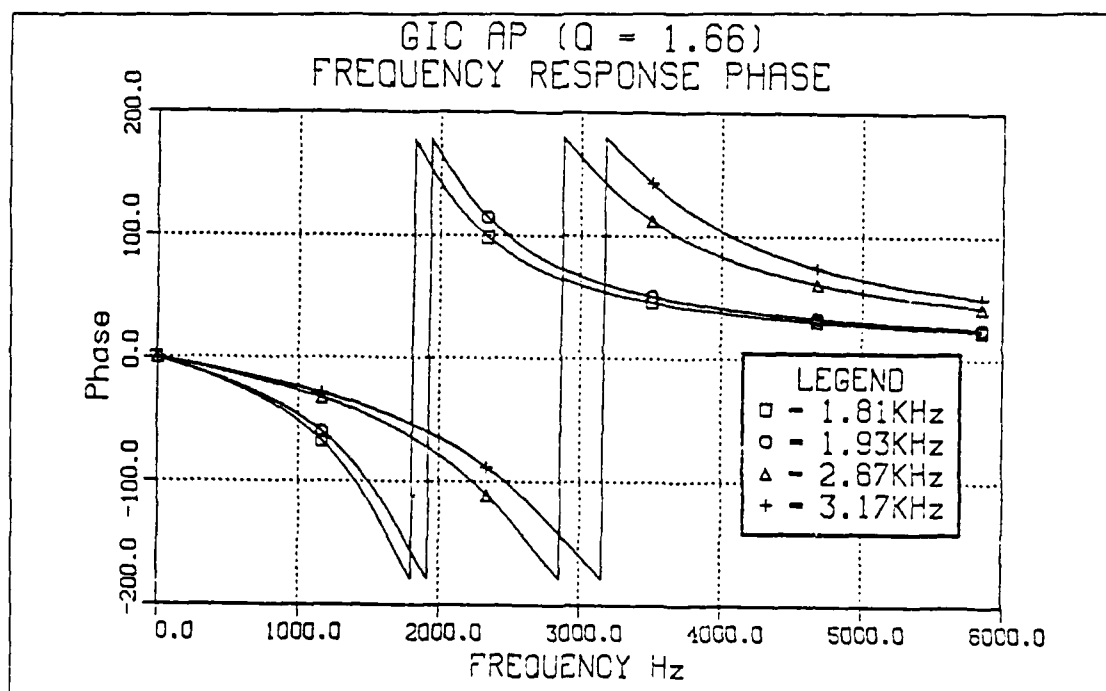


Figure 4.14 Ideal GIC AP Phase Response.

V. EXPERIMENTAL RESULT OF THE PROGRAMMABLE GIC SC FILTER

A. GENERAL

All parts of the circuit, of which detailed designs were shown in Chapter III, were integrated to construct the complete digitally controlled programmable GIC SC filter. After the circuit was built a variety of measurements were taken in order to study the response of the network with the different configuration, as explained in Chapter III. The switches in this GIC SC filter, are divided into two sets, each performing a different function. The first set of switches are used to control the filter characteristics. The second set are used for resistor realization using the switched capacitor techniques discussed earlier. The effect of the control switches which introduce a resistance of 80 ohm each at closed position can be found in [Ref. 6]. There are some general problems which may cause changes in the response of the network. These are listed below.

1. The prototype board creates capacitance values in the order of pfs at each node.
2. The master clock was provided by the EXACT MODEL 120 waveform generator which is not so stable. Its output varies with the time.
3. All switches introduce a resistance value from 60 ohm to 90 ohm at closed position.
4. All probes being used for measurement have some capacitance value.
5. Grounding problem.
6. The equipment scaling problem exists during the measurements.
7. Capacitor values change within their tolerance limitation.

In order to compare the experimental result to the computer simulation graphs, the closest control bitwords were used to set up the pole frequency and quality factor. After the response of all filter configurations were plotted, the clock frequency was varied to observe changes of pole frequency and the amount of linearity between clock and pole frequency. Finally, measurements were taken to show the sensitivity the quality factor to clock frequency changes.

B. LOW PASS FILTER

With the topology-control bitword 000, the network realized a Low Pass Filter response. Although all calculations were made under 101 KHz clock frequency, because of the unstability of the waveform generator mentioned above, average clock frequency

was found to be 99.5 KHz. Q_p was set to 1010 which corresponds to approximately 1.66. Magnitude response curves were plotted within the range of programmability of pole frequency, namely from 1.81 KHz to 30.3 KHz. Expected results were obtained up to 7.55 KHz. Beyond this frequency, the gain declined slightly, while quality factor experienced little changes. This can be seen in Figure 5.1 through 5.3. Control bitword for pole frequency was set to 1010, which is $f_p = 2.5$ KHz, while changing Q_p control bitword to 1000, 0101 and, 0011 which corresponds to 2.11, 4.07 and, 5.19 respectively. Figure 5.4 was plotted under these conditions. The plot is quite similar to computer simulation except $Q_p = 5.19$. This is also expected because of the fact that setting up the quality factor to 5.19 requires 440 pf capacitance value. This value falls out of the range that we considered in Figure 1.15. The continuous resistance value was not realizable according to the design value. As a result, some deviation from quality factor was experienced. Figure 5.4 shows that the pole frequency was not effected, since the 440 pf capacitor is not the element used to control f_p .

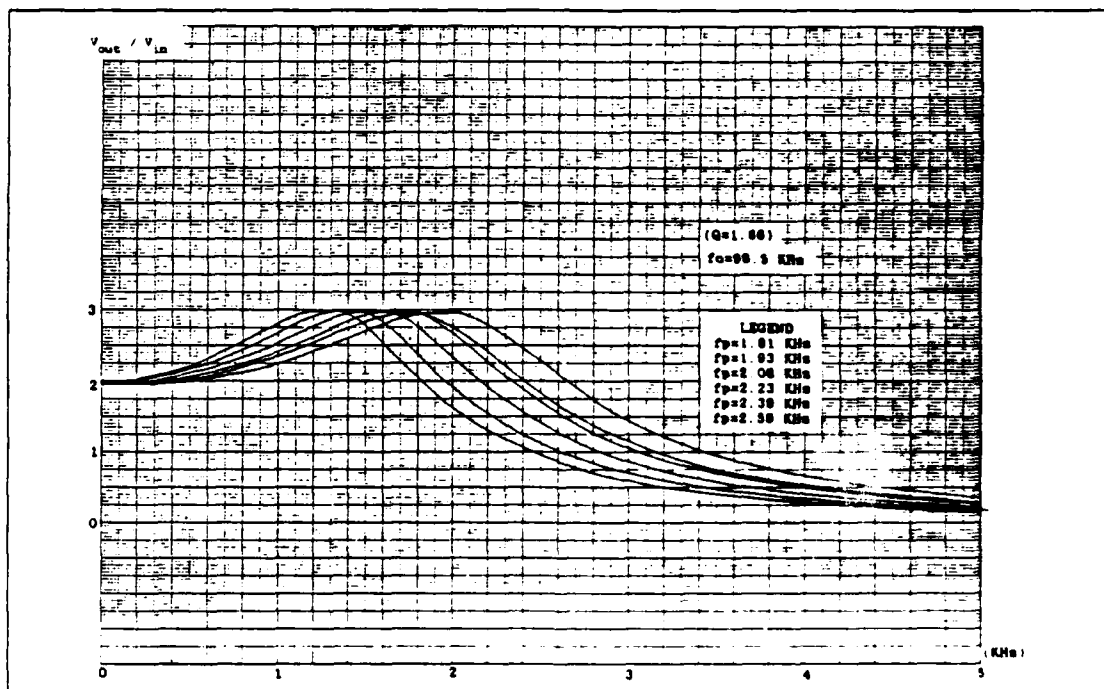


Figure 5.1 Experimental Result of LPF with Different f_p .

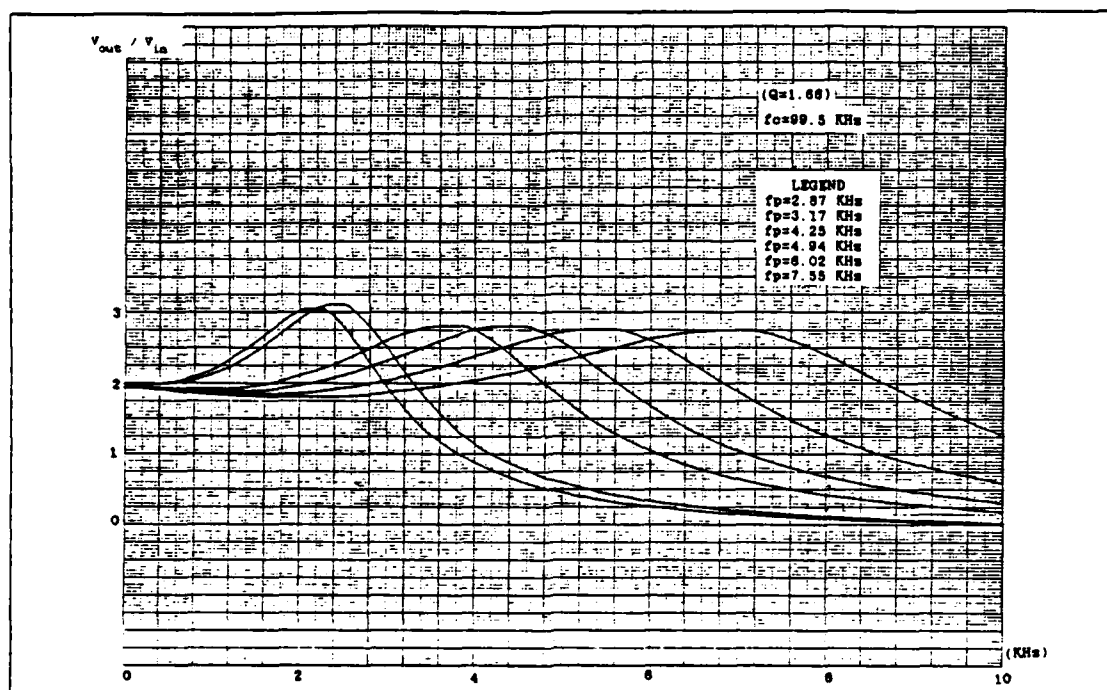


Figure 5.2 Experimental Result of LPF with Different f_p .

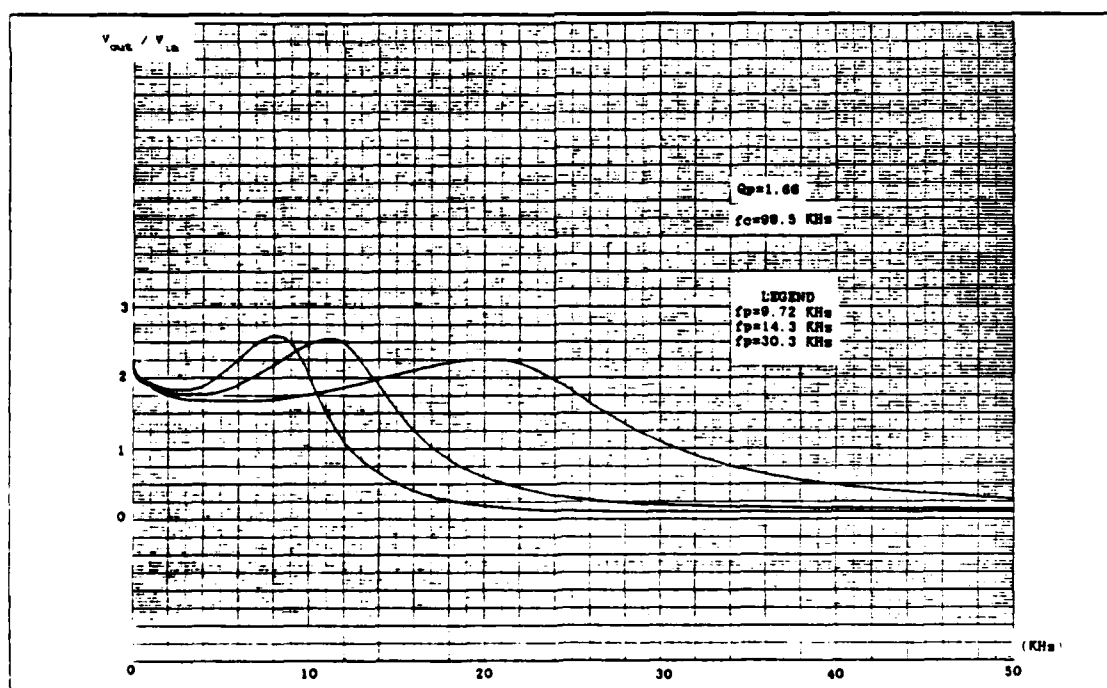


Figure 5.3 Experimental Result of LPF with Different f_p .

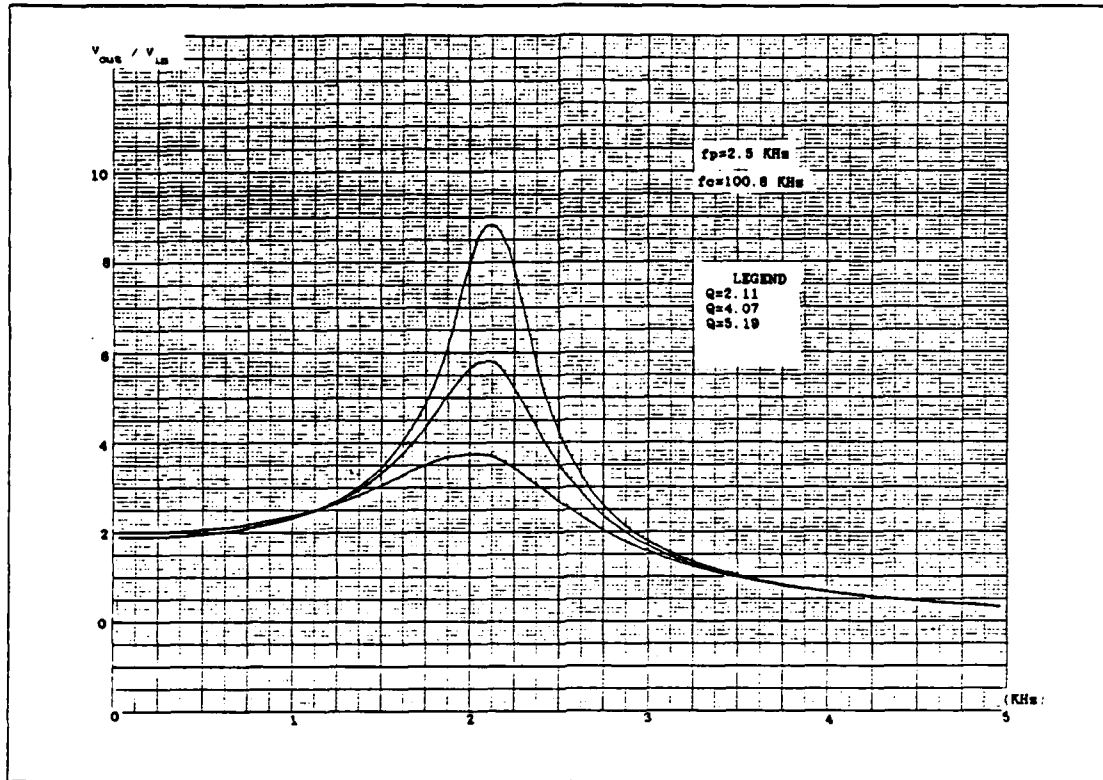


Figure 5.4 Experimental Result of LPF with Different Q_p .

C. HIGH PASS FILTER

With the topology-control bitword 001, the network realized a High Pass Filter. For this case, all measurements are taken under 101.8 KHz clock frequency. The quality factor was set to 1.66 for six different values of pole frequency shown in Figure 5.5 through Figure 5.7. In regard to pole frequency and gain, expected results were obtained. But the quality factor tends to get closer to computed curve up to 5 KHz frequency range and then diverges. On the other hand, if we consider changes in the quality factor, as shown in Figure 5.8, the small Q_p s were implemented more accurately. This is because, small quality factors require larger capacitance value and these values can realize the equivalent resistance well enough. Three different quality factors were used when Figure 5.8 was plotted. There is no distortion in the pole frequency as expected theoretically.

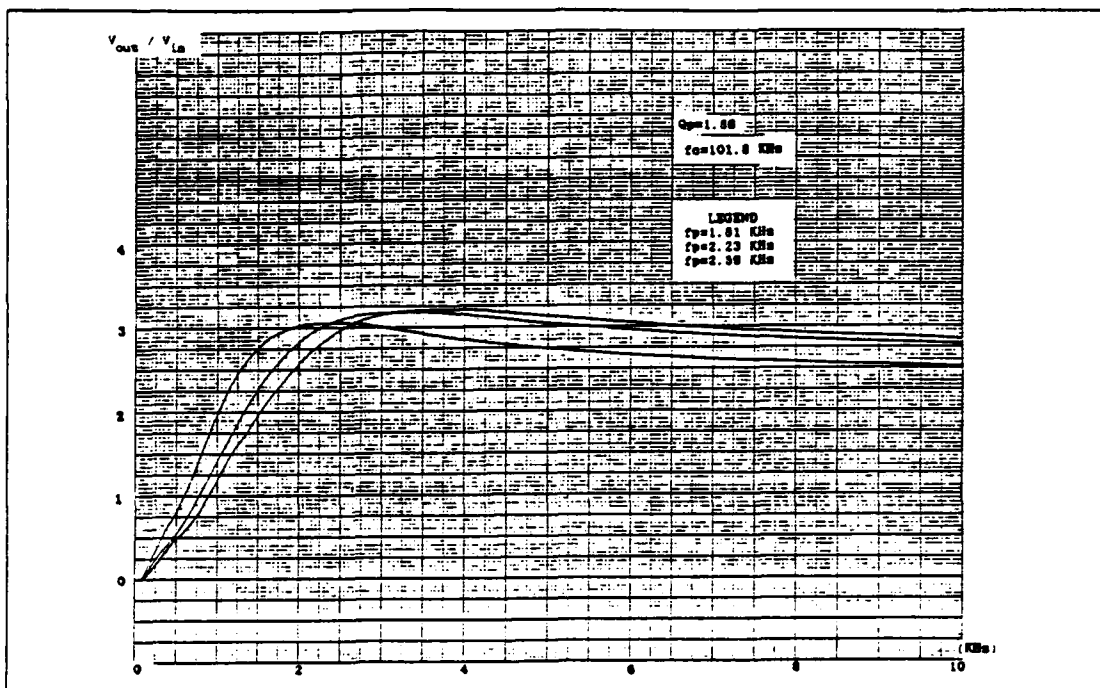


Figure 5.5 Experimental Result of HPF with Different f_p .

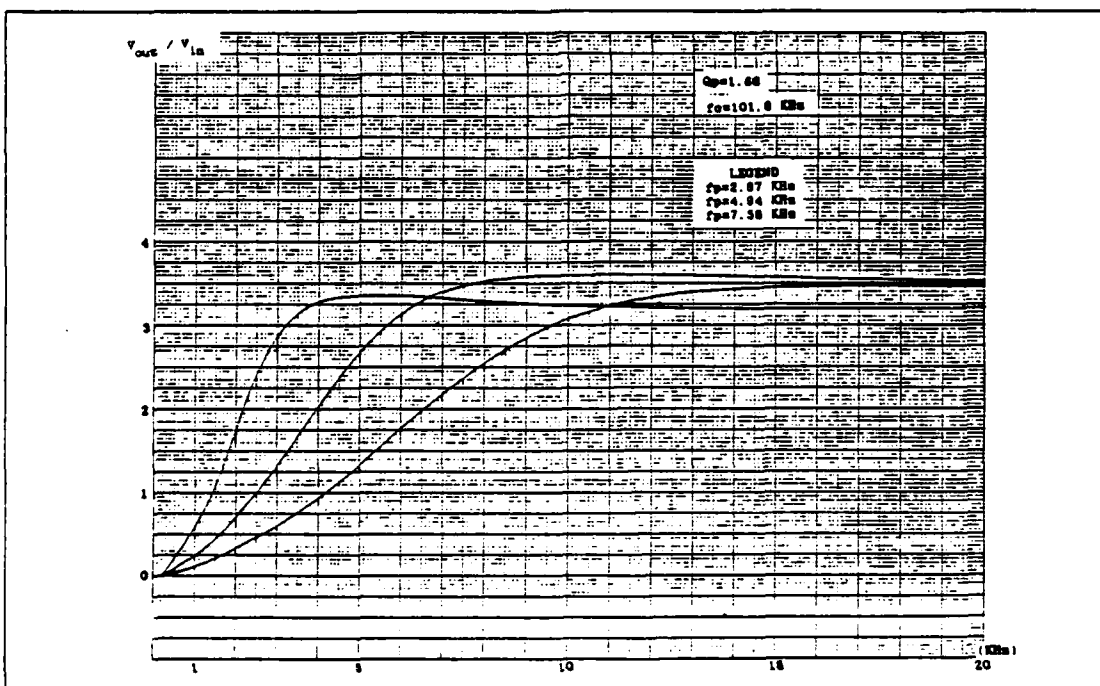


Figure 5.6 Experimental Result of HPF with Different f_p .

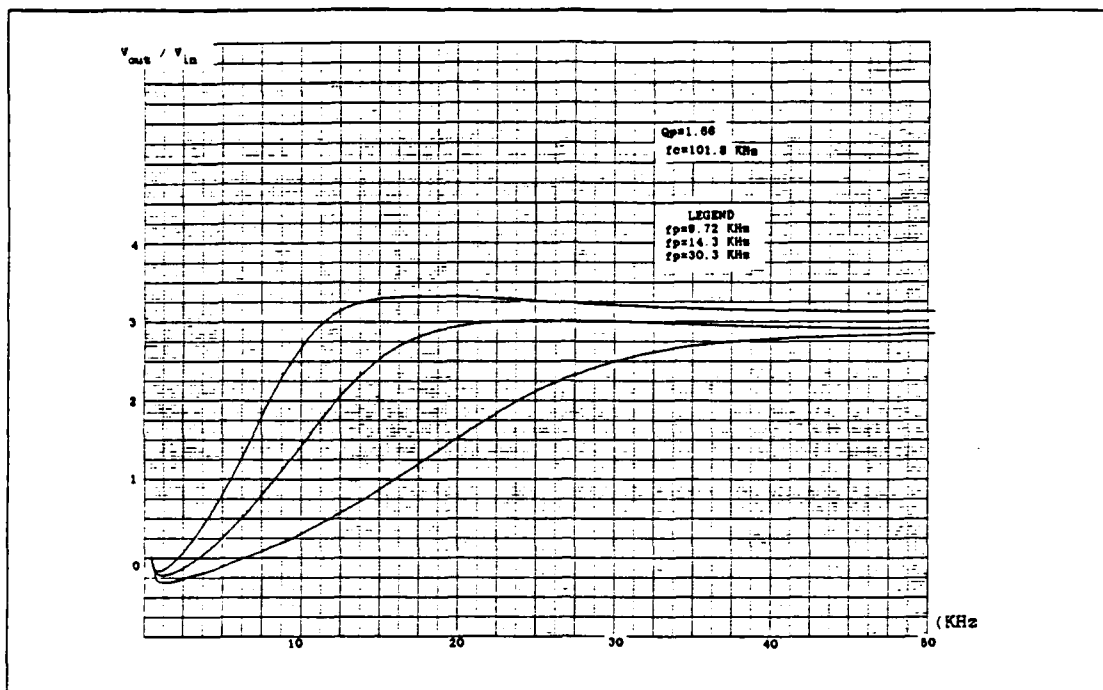


Figure 5.7 Experimental Result of HPF with Different f_p .

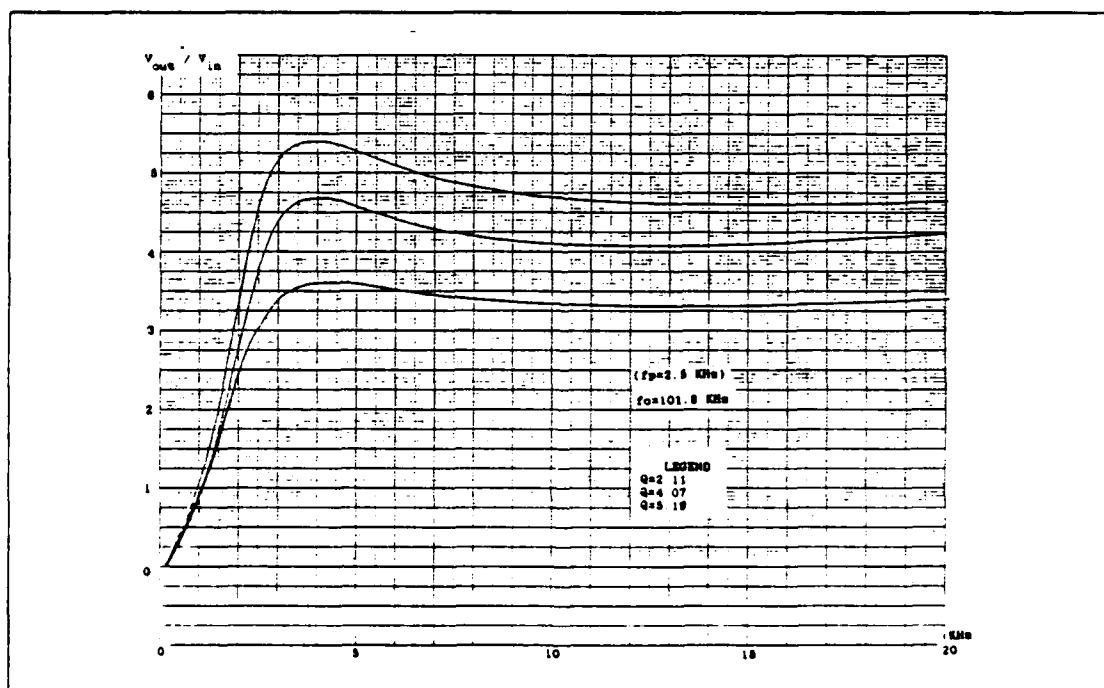


Figure 5.8 Experimental Result of HPF with Different Q_p .

D. BAND PASS FILTER

The 010 topology-control bitword realizes the Band Pass Filter. The quality factor was set to 0100 which corresponds to 4.52. Figure 5.9 and Figure 5.10 were plotted for various pole frequencies. The results agree with the computer simulations with minor amplitude fluctuations. Figure 5.11 was plotted at 2.59 KHz pole frequency for various quality factors, 5.19, 7.76, 15.5. An important observation on this figure is the fact that the quality factor increases, while the gain decreases. But again, similar to other cases, pole frequency remained constant. This situation is shown apparently in Figure 5.11.

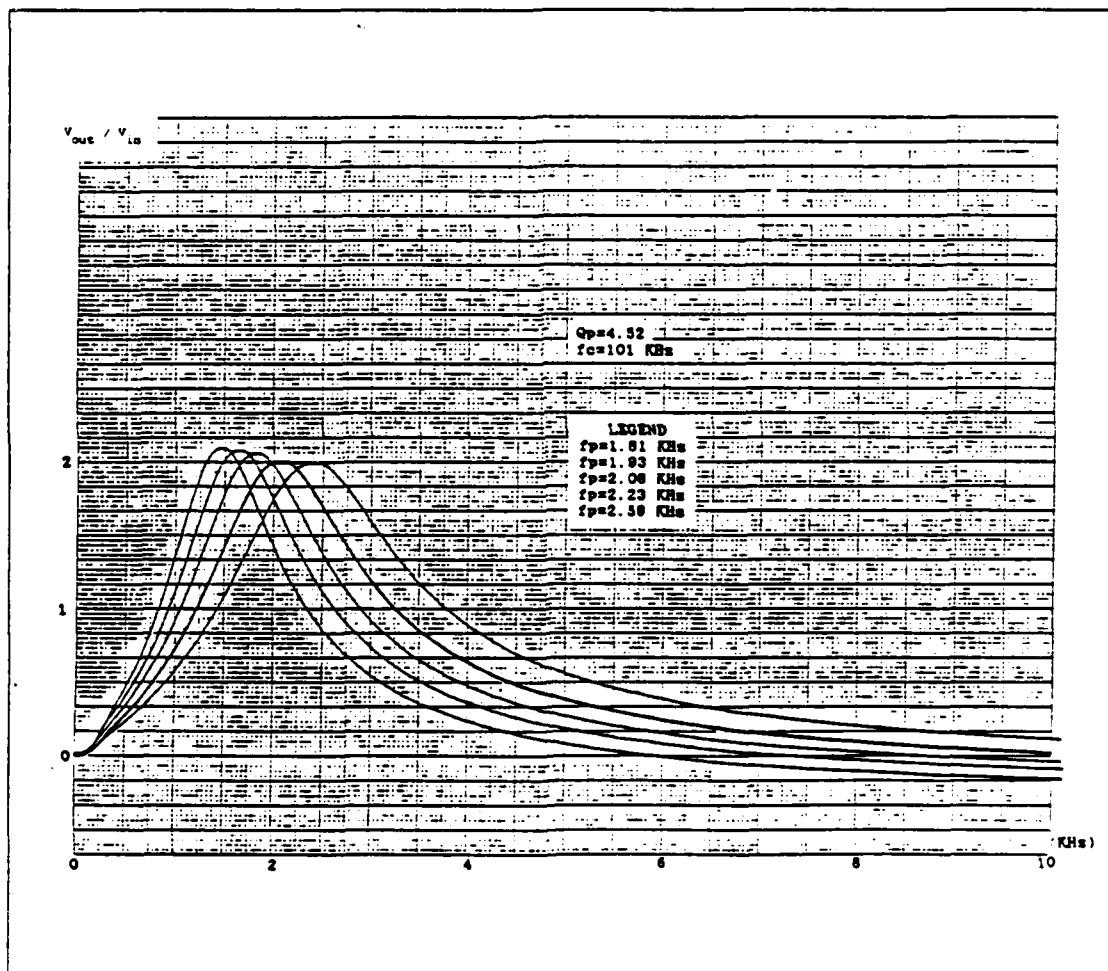


Figure 5.9 Experimental Result of BPF with Different f_p .

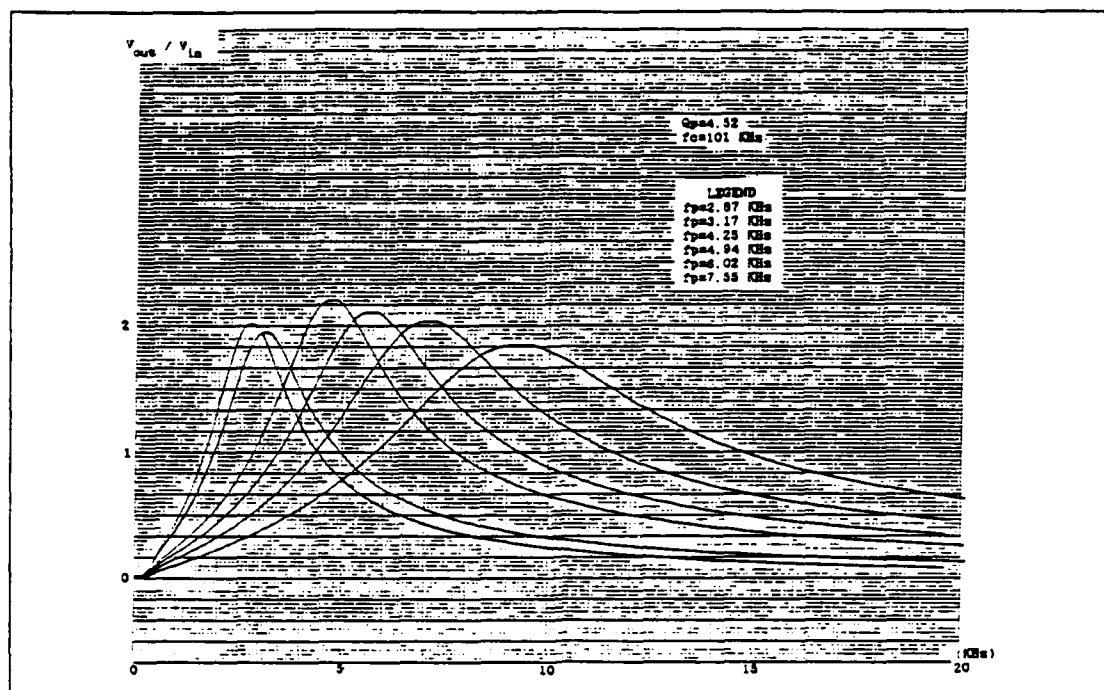


Figure 5.10 Experimental Result of BPF with Different f_p .

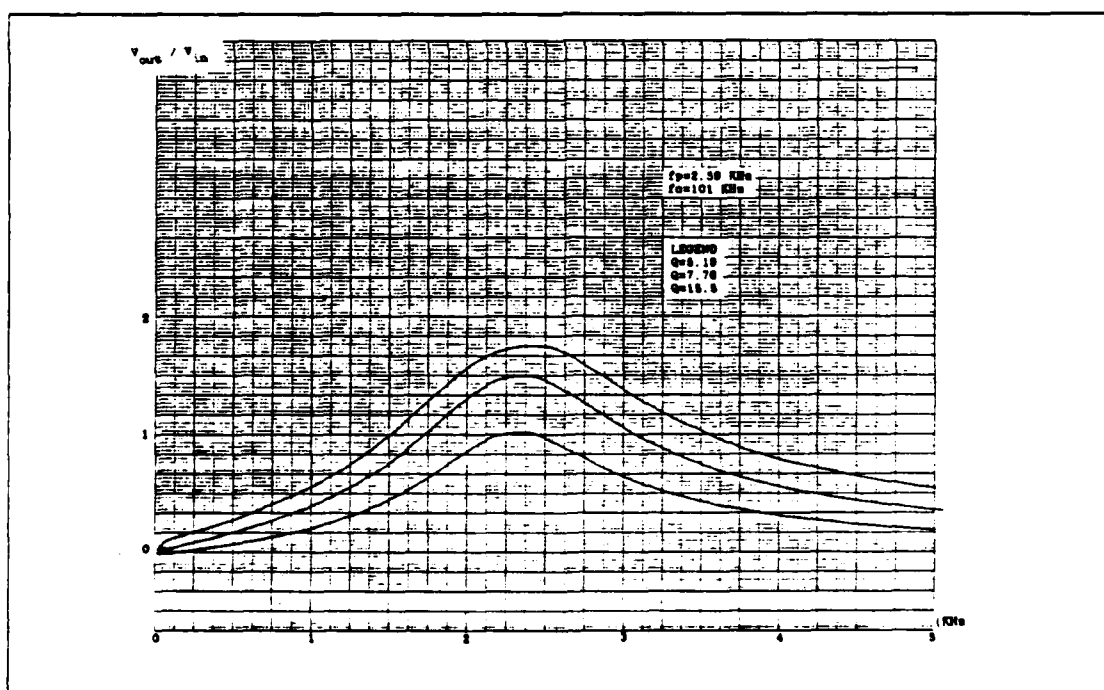


Figure 5.11 Experimental Result of BPF with Different Q_p .

E. NOTCH FILTER

With the topology-control bitword 011, a Notch Filter realization can be achieved. Figure 5.12 illustrates the amplitude response for different frequencies for $Q_p = 5.19$, while Figure 5.13 illustrates amplitude response for $f_p = 7.55$ KHz and a variety of quality factors. The above figures agree with the theoretical transfer function. Since the notch frequency, W_n , depends on the both pole frequency and quality factor, whenever pole frequency (or quality factor) changes, notch frequency and also quality factor (or pole frequency) reflect this variation as it is seen in Figure 5.12 and Figure 5.13.

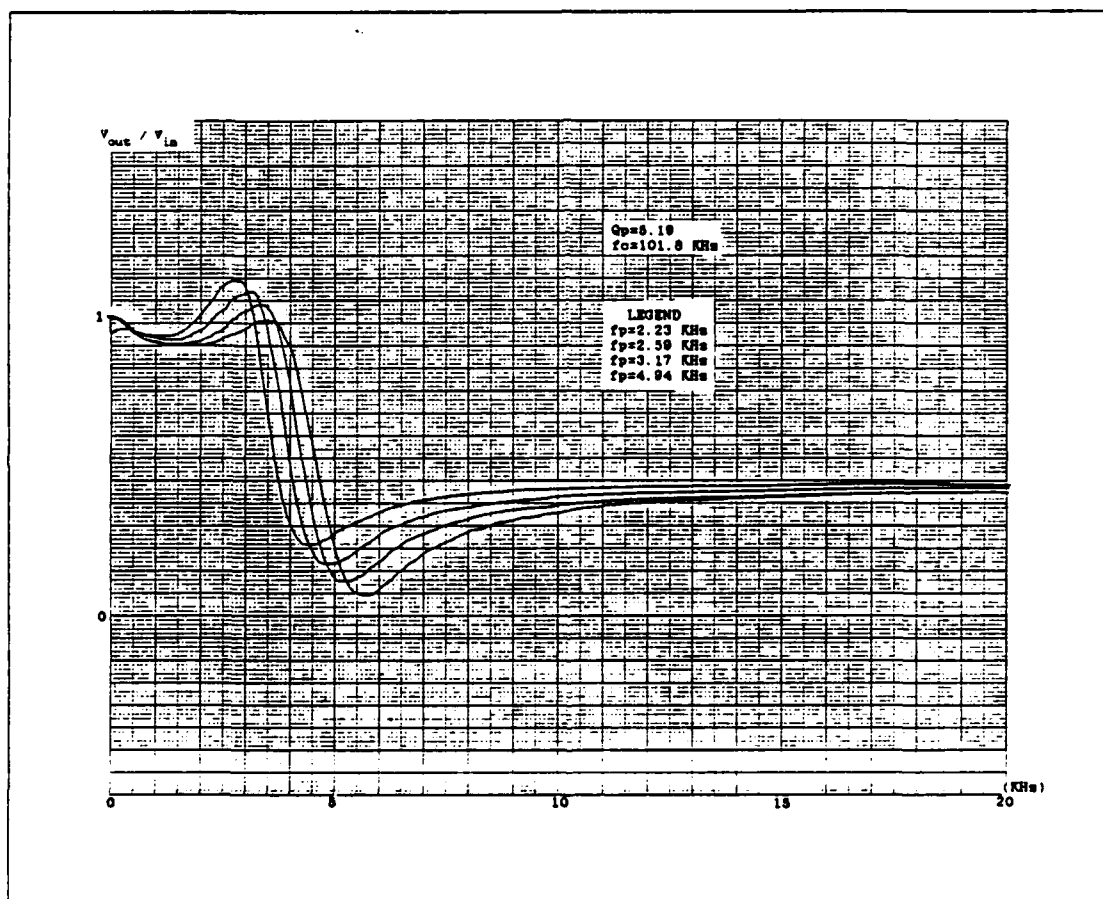


Figure 5.12 Experimental Result of NF with Different f_p .

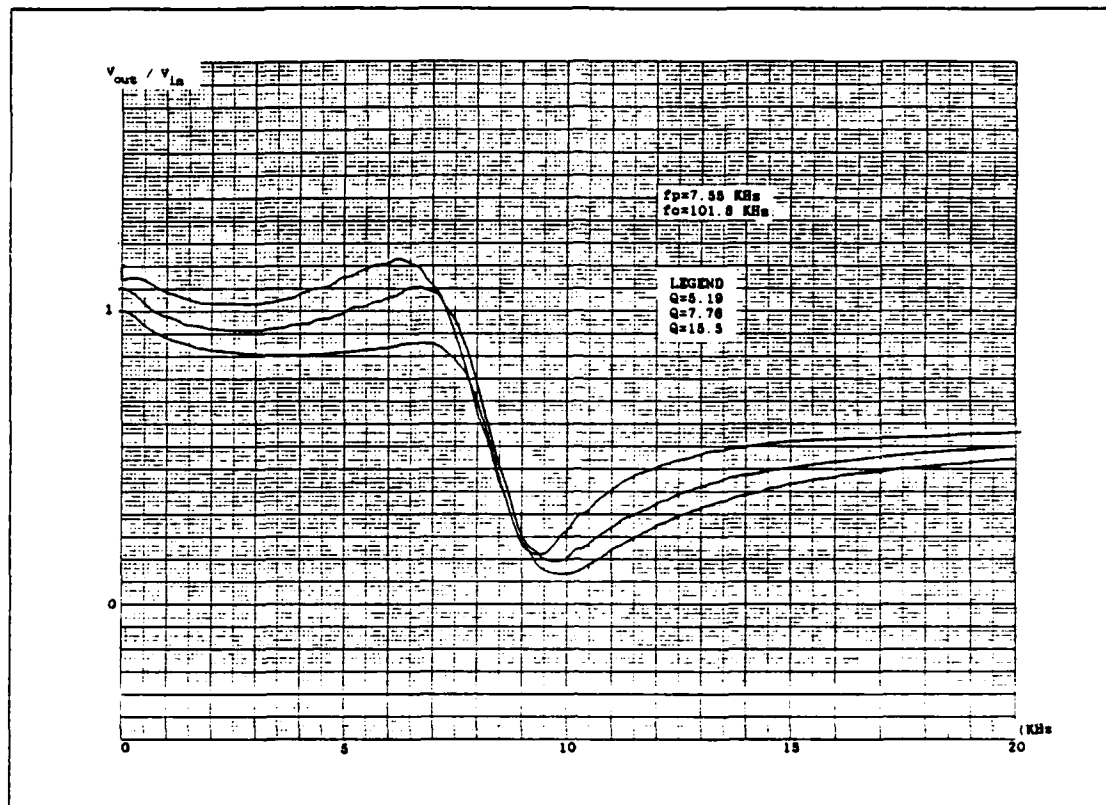


Figure 5.13 Experimental Result of NF with Different Q_p .

F. ALL PASS FILTER

The topology-control bitword 100 realizes an All Pass Filter. Figure 5.14 illustrates frequency response of the realized all pass filter for different pole frequency while quality factor is held constant. For this particular filter, 360° phase shift was observed at the pole frequency which agrees with the computer simulation.

G. EFFICIENCY OF THE CLOCK FREQUENCY

In order to observe the affect of the clock frequency, f_c , two different plots have been taken. As mentioned in Chapter III, if the clock frequency changes by some constant α , the pole frequency shifts by an amount which is related to this constant α . The programmable filter can be programmed to almost any frequency (from 1 KHz to 60 KHz) by using this feature. Figure 5.15 shows this property, where the first LPF uses 50.97 KHz while the second is using 103.5 KHz. This means that the clock frequency changed almost 50 KHz, correspondingly pole frequency shifted almost 0.75

KHz. The last three LPF curves in Figure 5.15 had 103.5 KHz, 201 KHz and, 299.5 KHz clock frequency. The difference from each other was almost 100 KHz, correspondingly the pole frequencies differ from each other almost 1.5 KHz which proves the concept stated above.

Finally, the affect of the clock frequency with respect to quality factor, Q_p , will be demonstrated. In order to do so, first pole frequency was set to 1111, 1.81 KHz by using 103.25 KHz clock frequency (curve 1 in Figure 5.16) then pole frequency, f_p , was changed to 4.25 KHz using control bitword 0111 with same clock frequency (curve 2 in Figure 5.16). From this f_p , the clock frequency was decreased until the same f_p was realized as in curve 1. This was plotted as curve 3 in Figure 5.16. By comparing curve 1 and curve 3 one can observe that there is no major changes in terms of quality factor. This can prove experimentally the low sensitivity of the quality factor Q_p , to the clock frequency variations.

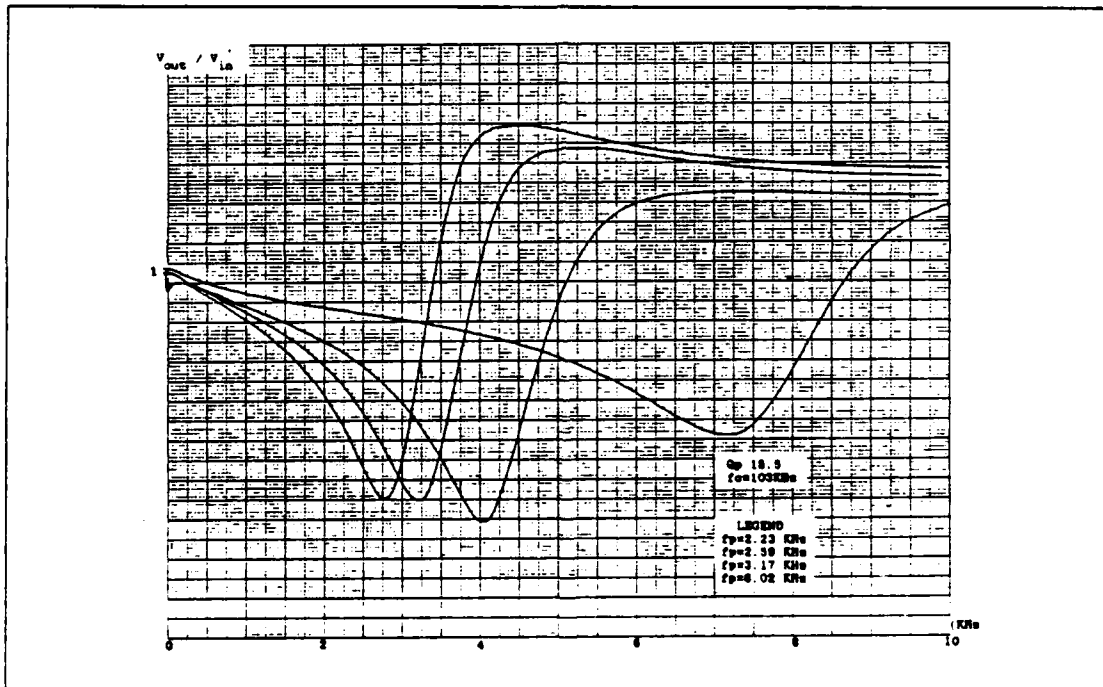


Figure 5.14 Experimental Result of AF with Different f_p .

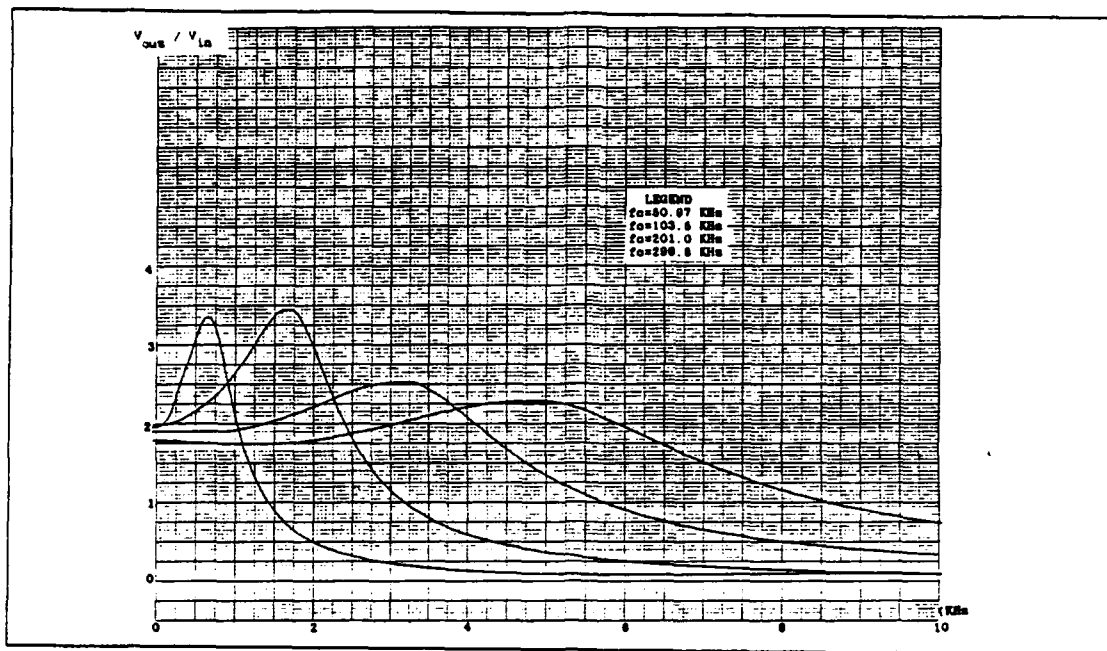


Figure 5.15 Experimental Result Showing the Effect of the f_c .

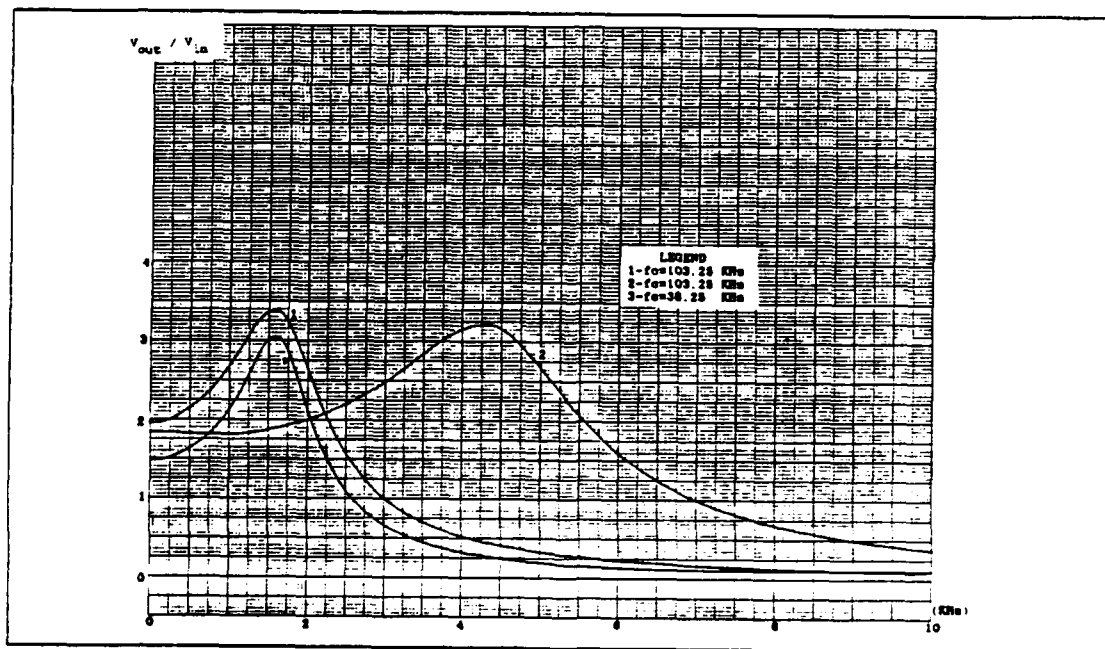


Figure 5.16 Experimental Result Showing the Effect of the f_c .

VI. CONCLUSION

The design described here has resulted in a universal programmable switched capacitor filter that can be digitally controlled to realize almost any practical filter specifications. This is done through the use of CMOS switches controlled by binary codes to program the filter topology, the filter center frequency, quality factor. The bilinear switched capacitor realization of a continuous resistor was used as a key concept of the research. The design procedure required developing optimum switching arrangements for the minimum redundancy in components and least dependence of the filtering function on switching imperfections such as switches stray capacitances and non-zero and nonlinear switch-on resistance. Further investigation is needed eliminate the effect of the stray capacitance introduced by the switched capacitors. The sensitivity of Q_p is found to be low with respect to clock frequency. The clock frequency could also be used to program the filter by scaling the center frequencies through different ranges. The experimental results showed close agreement between theory and practice. Further, these results indicate that these realizations are insensitive to temperature and power supply variations.

This study can be extended for developing a wide bandwidth programmable switched capacitor filter using the composite operational amplifier technique proposed by [Ref. 9]. Such implementation would lead to a very useful monolithic device at moderate cost.

This research can be also brought into the subject of VLSI design to implement the whole network structure into the single custom chip, which is the final goal of the research.

APPENDIX A

TRANSFORMATION PROGRAM

```

SSTORAGE:2
  REAL A0,A1,A2,B0,B1,B2,K,F,A,SP,DELTH
  REAL AZ0,AZ1,AZ2,BZ0,BZ1,BZ2
  SP = 0.0
  DELTH = 0.0062831853
  N = 2
  M = 2
  NP = 501
  BZ0 = 1.0
  WRITE(*,*) 'THIS PROGRAM TRANSFORMS SECOND-ORDER S-DOMAIN TRANSFER'
  WRITE(*,*) 'FUNCTION TO Z-DOMAIN TRANSFER FUNCTION USING BILINEAR'
  WRITE(*,*) 'MAPPING METHOD.WT/2 << 1 IS ASSUMED.'
  WRITE(*,*) 'IF YOU ARE DEALING WITH THE SC CIRCUIT, YOU HAVE TO'
  WRITE(*,*) 'TAKE SAMPLING FREQUENCY AS TWICE AS MUCH ITSELF.'
  WRITE(*,*) ' '
  WRITE(*,*) 'ENTER THE SAMPLING FREQUENCY IN HZ.'
  READ(*,*) F
  WRITE(*,*) '(A0*S**2)+(A1*S)+A2 IS THE FORM OF NUMARETOR'
  WRITE(*,*) 'ENTER A0,A1,A2'
  READ(*,*) A0,A1,A2
  WRITE(*,*) '(B0*S**2)+(B1*S)+B2 IS THE FORM OF THE DENOMINATOR'
  WRITE(*,*) 'ENTER B0,B1,B2'
  READ(*,*) B0,B1,B2
  K = 2.0*F
  A = (32+(B1*K)+(B0*K**2))
  AZ0 = (A2+(A1*K)+(A0*K**2))/A
  AZ1 = ((2.0*A2)-(2.0*A0*K))/A
  AZ2 = (A2-(A1*K)+(A0*K**2))/A
  BZ1 = ((2.0*B2)-(2.0*(B0*K**2)))/A
  BZ2 = (B2-(B1*K)+(B0*K**2))/A
  OPEN(8,FILE='BILINEAR.DAT',STATUS='NEW')
  WRITE(8,101) N,M,NP,SP,DELTH
  WRITE(8,102) AZ0
  WRITE(8,102) AZ1
  WRITE(8,102) AZ2
  WRITE(8,102) BZ0
  WRITE(8,102) BZ1
  WRITE(8,102) BZ2
  CLOSE(8)

SPACE
  WRITE(*,*) 'H(Z) = ((AZ0*Z**2)+(AZ1*Z)+AZ2)/((Z**2)+(BZ1*Z)+BZ2)'
  WRITE(*,101) N,M,NP,SP,DELTH
  WRITE(*,103) AZ0
  WRITE(*,104) AZ1
  WRITE(*,105) AZ2
  WRITE(*,106) BZ0
  WRITE(*,107) BZ1
  WRITE(*,108) BZ2
101  FORMAT(2I3,2X,I4,2(4X,F13.10))
102  FORMAT(3X,F13.10)
103  FORMAT(3X,'AZ0 = ',F13.10)
104  FORMAT(3X,'AZ1 = ',F13.10)
105  FORMAT(3X,'AZ2 = ',F13.10)
106  FORMAT(3X,'BZ0 = ',F13.10)
107  FORMAT(3X,'BZ1 = ',F13.10)
108  FORMAT(3X,'BZ2 = ',F13.10)
  STOP
  END

```

APPENDIX B

SIMULATION PROGRAM

```

C THIS PROGRAM CALCULATES THE FREQUENCY RESPONSE OF A CONTINUOUS ...
C ...SYSTEM. THE INPUT IS A RATIO OF TWO POLYNOMIALS OF THE FORM ...
C
C      (B(0)*S**M + B(1)*S**(M-1) + ... + B(M-1)*S + B(M)) /
C      (A(0)*S**N + A(1)*S**(N-1) + ... + A(N-1)*S + A(N))
C
C WHERE THE NUMERATOR COEFFICIENTS B(0), B(1), ..., B(M) AND THE ...
C ... THE DENOMINATOR COEFFICIENTS A(0), A(1), ..., A(N) ARE REAL ...
C ... NUMBERS AND THE DEGREE OF THE NUMERATOR POLYNOMIAL, M, AND ...
C ... THE DEGREE OF THE DENOMINATOR POLYNOMIAL, N, ARE POSITIVE ...
C ... INTEGERS. THE A'S, B'S, M, AND N ARE READ IN AS DATA, AS IS ...
C ... OMEGA0 (THE STARTING VALUE OF OMEGA IN RADIANS) ...
C ... OMEGA IS DEFINED BY S = J*OMEGA DLOMGA (THE ...
C ... INCREMENT OF OMEGA), AND NUMPTS (THE NUMBER OF POINTS)
C
C      IT IS ASSUMED THAT ALL SYSTEM POLES HAVE NEGATIVE REAL PARTS.
C
C      INTEGER M,N,NUMPTS
C      COMPLEX S,DEN,NUM,H,CI
C      REAL MH(1000),PH(1000),OMEGAV(1000),A(128),B(128),IMS,RES,DLOMGA
C      CALL TEK618
C      CALL SHERPA('IKISEKI ','A',3)
C      CALL BLOWUP(0.75)
C      CALL PAGE(9.0,5.5)
C      CALL HWROT('AUTO')
C      CALL NOBRDR
C      CALL HEIGHT(0.15)
C      CALL MX1ALF('STANDARD','&')
C      CALL MX2ALF('L/CSTD','#')
C      CALL MX3ALF('GREEK','%')
C      CALL MX4ALF('L/CGREEK','@')
C      NP = 0
C      NPROP = 1
1     READ(4,1000) M,N,DLOMGA,OMEGAO,NUMPTS
C      NP = NP+1
C      WRITE(8,1008)
C      WRITE(8,1110) M
C      WRITE(8,1111) N
C      WRITE(8,1112) NUMPTS
C      WRITE(8,1113) OMEGA0
C      WRITE(8,1114) DLOMGA
C      IT IS ASSUMED THAT DLOMGA IS READ IN IN RADIANS/SEC
C      PI=3.141592654
C      MP1=M+1
C      NP1=N+1
C      READ(4,1001) (B(I),I=1,MP1)
C      READ(4,1001) (A(I),I=1,NP1)
C      WRITE(8,1004)
C      WRITE(8,1005) (B(I),I=1,MP1)
C      WRITE(8,1006)
C      WRITE(8,1005) (A(I),I=1,NP1)
C      CI = (1.,0.)
C
C      BEGIN MAIN LOOP
C
C      DO 100 L=1,NUMPTS
C          NUM = CI*B(1)

```

```

      DEN = CI*A(1)
C    UPDATE VALUE OF OMEGA
      OMEGA = OMEGA0 + (L-1)*DLOMGA
      OMEGAV(L) = OMEGA/(2.*PI)
      RES = 0.0
      IMS = OMEGA
      S = CMPLX(RES,IMS)
      IF(M.EQ.0) GO TO 60
      DO 50 J = 1,M
50    NUM = S*NUM + CI*B(J+1)
60    CONTINUE
      IF(N.EQ.0) GO TO 80
      DO 70 J = 1,N
70    DEN = S*DEN + CI*A(J+1)
80    CONTINUE
      H = NUM/DEN
      MH(L) = CABS(H)
      IF(ABS(REAL(H)).GE.1.E-15) GO TO 90
      IF(ABS(IMAG(H)).LE.1.E-15) PH(L) = 0.0
      IF(IMAG(H).GT.1.E-15) PH(L) = PI/2.
      IF(IMAG(H).LT.-1.E-15) PH(L) = -PI/2.
      GO TO 95
90    PH(L) = ATAN2(IMAG(H),REAL(H))
95    PH(L) = PH(L)*180./PI
100  CONTINUE
      WRITE(8,1009)
      WRITE(8,1002)
      WRITE(8,1007)
      DO 150 L=1,NUMPTS
150  WRITE(8,1003)OMEGAV(L),MH(L),PH(L)
1000 FORMAT(2(I3,7X),2(E10.4),I3)
1001 FORMAT(8(E10.4))
1002 FORMAT(///,8X,'OMEGA',7X,'MAGNITUDE(M)',6X,'PHASE(P)')
1007 FORMAT(8X,'RAD/S',23X,'DEGREES',/)
1003 FORMAT(3(2X,E14.6))
1004 FORMAT(2X,'THE NUMERATOR COEFFICIENTS B(0),B(1),...,B(M) ARE',/)
1005 FORMAT(10(1X,E11.4),/)
1006 FORMAT(//,2X,'THE DENOMINATOR COEFFICIENTS A(0),A(1),...A(N) ARE',
*)
1008 FORMAT(20X,' INPUT DATA ',///)
1009 FORMAT(////////,20X,' OUTPUT DATA ',///)
1010 FORMAT(2(2X,E11.4,///))
1110 FORMAT(2X,'DEGREE OF NUMERATOR = ',I3)
1111 FORMAT(2X,'DEGREE OF DENOMINATOR = ',I3)
1112 FORMAT(2X,'NUMBER OF FREQUENCY POINTS = ',I4)
1113 FORMAT(2X,'STARTING VALUE OF OMEGA = ',E12.6)
1114 FORMAT(2X,'INCREMENT OF OMEGA = ',E12.6,/)
C
C    ***** DISSPLAY *****
C    CALL COMPRS
      XMIN = OMEGA0
C    XMAX = OMEGAV(NUMPTS)
      XMAX = 5000.
      XINC = XMAX/20.
      MAGMAX = -0.05
      MAGMIN = 0.0
      PHMAX = -1.E15
      PHMIN = 1.E15
      DO 180 I = 1, NUMPTS
      IF(MH(I).GT.MAGMAX) MAGMAX = MH(I)
      IF(PH(I).GT.PHMAX) PHMAX = PH(I)
      IF(MH(I).LT.MAGMIN) MAGMIN = MH(I)
180  IF(PH(I).LT.PHMIN) PHMIN = PH(I)
C    GO TO(210,220,220,220),NP
      GO TO(210,220,220,220,220),NP
210  CONTINUE
      CALL AREA2D(6.0,3.5)
      CALL XNAME('FREQUENCY H#Z&S',100)
      CALL YNAME('MAGNITUDE S',100)

```

```

CALL HEADIN(' $',100,1.2,4)
CALL HEADIN(' $',100,1.2,4)
CALL HEADIN(' R1 = 21.77K C2 = 431#P&F R3 = 1.17M$',100,1.2,4)
CALL HEADIN(' FREQUENCY RESPONSE MAGNITUDES',100,1.2,4)
CALL CROSS
C CALL XNONUM
CALL GRAF(XMIN,'SCALE',XMAX,0.,'SCALE',MAGMAX)
C CALL GRAF(XMIN,'SCALE',XMAX,0.,0.5,2.5)
C X1=MAGMAX/14.
CALL HEIGHT(0.2)
C CALL RLMESS('%Q&$',100,3.2,0.0)
C CALL HEIGHT(0.15)
C CALL RLMESS('@P &$',100,-3.27,-X1)
C CALL RLMESS('-3@P&/4$',100,-2.60,-X1)
C CALL RLMESS('@P&/2$',100,-1.77,-X1)
C CALL RLMESS('-@P&/4$',100,-0.98,-X1)
C CALL RLMESS('0$',100,-0.037,-X1)
C CALL RLMESS('@P&/4$',100,0.68,-X1)
C CALL RLMESS('@P&/2$',100,1.47,-X1)
C CALL RLMESS('3@P&/4$',100,2.22,-X1)
C CALL RLMESS('@P&$',100,3.10,-X1)
C CALL MARKER(15)
220 CALL CURVE(OMEGAV,MH,NUMPTS,0)
C CALL AREA2D(6.0,3.5)
C CALL XNAME('FREQUENCY H#Z&$',100)
C CALL YNAME('P#HASE&$',100)
C CALL HEADIN(' $',100,1.2,4)
C CALL HEADIN(' $',100,1.2,4)
C CALL HEADIN(' LOSSLESS INTEGRATOR $',100,1.2,4)
C CALL HEADIN(' R1 = 21.77K C2 = 431#P&F R3 = 1.17M$',100,1.2,4)
C CALL HEADIN(' GIC AP (Q = 1.66) $',100,1.2,4)
C CALL HEADIN(' FREQUENCY RESPONSE PHASE $',100,1.2,4)
CALL CROSS
CALL GRAF(XMIN,XINC,XMAX,PHMIN,'SCALE',PHMAX)
CALL GRAF(XMIN,'SCALE',XMAX,PHMIN,'SCALE',PHMAX)
X2=(PHMAX-PHMIN)/16.
CALL HEIGHT(0.2)
CALL RLMESS('%Q&$',100,3.2,0.0)
CALL HEIGHT(0.15)
CALL RLMESS('@P &$',100,-3.27,-X2)
CALL RLMESS('-3@P&/4$',100,-2.60,-X2)
CALL RLMESS('@P&/2$',100,-1.77,-X2)
CALL RLMESS('-@P&/4$',100,-0.98,-X2)
CALL RLMESS('0$',100,-0.037,-X2)
CALL RLMESS('@P&/4$',100,0.68,-X2)
CALL RLMESS('@P&/2$',100,1.47,-X2)
CALL RLMESS('3@P&/4$',100,2.22,-X2)
CALL RLMESS('@P&$',100,3.10,-X2)
CALL CURVE(OMEGAV,PH,NUMPTS,0)
CALL RESET('CROSS')
CALL ENDPL(0)
IF(NP.LT.NPROP) GOTO 1
CALL LINES('1.81KH#Z&$',IPAK,1)
CALL LINES('1.93KH#Z&$',IPAK,2)
CALL LINES('2.87KH#Z&$',IPAK,3)
CALL LINES('3.17KH#Z&$',IPAK,4)
XW = XLEGND(IPAK,4)
YW = YLEGND(IPAK,4)
XL = 6.2-.5-XW-.1
YL = 2.3-.5-YW-.1
CALL BLNK1(XL-.1,6.2-.5,YL-.1,2.3-.5,2)
CALL DOT
CALL GRID(1,1)
CALL RESET('DOT')
CALL RESET('BLNK1')
CALL LEGEND(IPAK,4,XL,YL)
CALL ENDPL(0)
CALL DONEPL

```


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9-87

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